
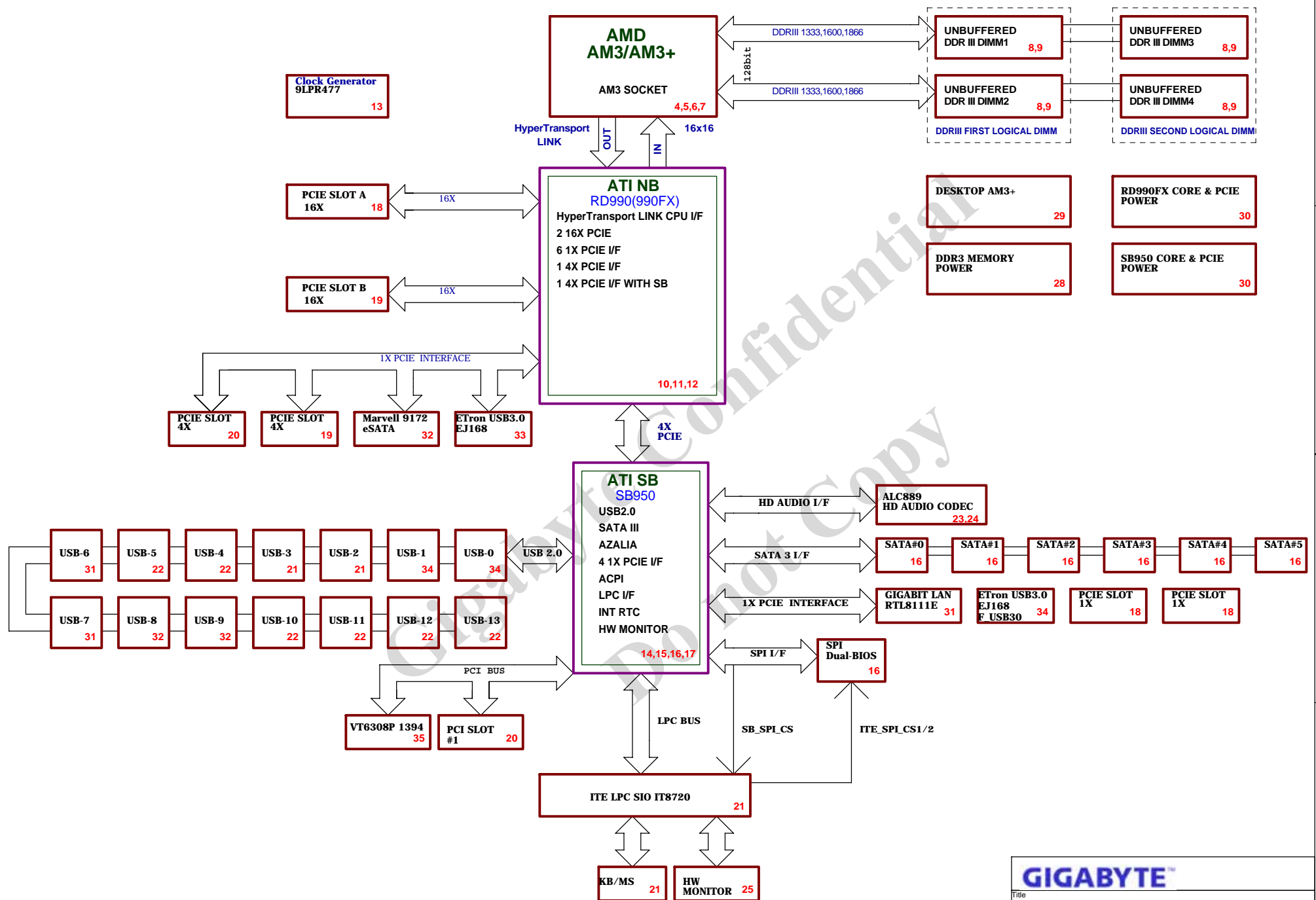


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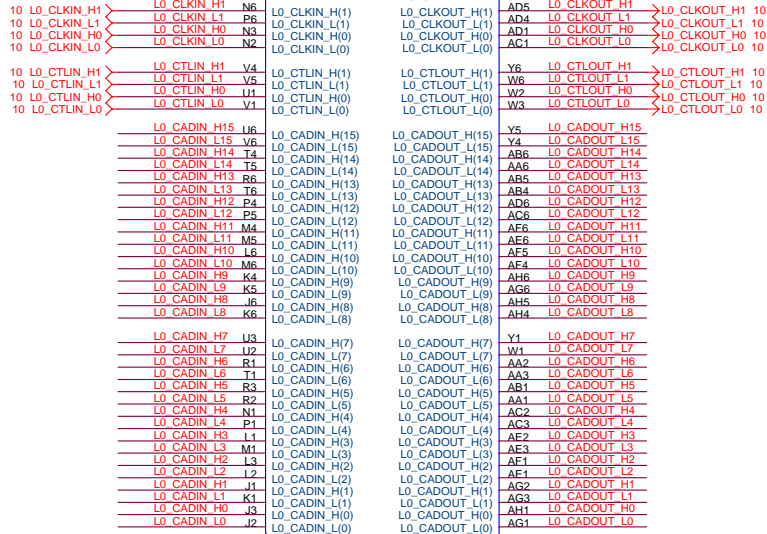
BLOCK DIAGRAM

Size	Document Number	Rev
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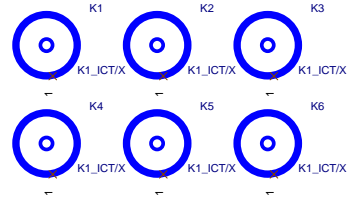
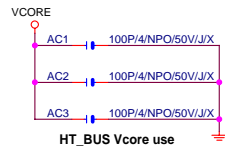
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 L0_CADIN_H[0..15] <L0_CADIN_H[0..15] 10
 L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] 10
 L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] 10

M2CPUA

HYPERTRANSPORT

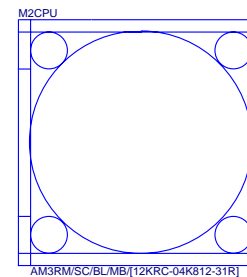
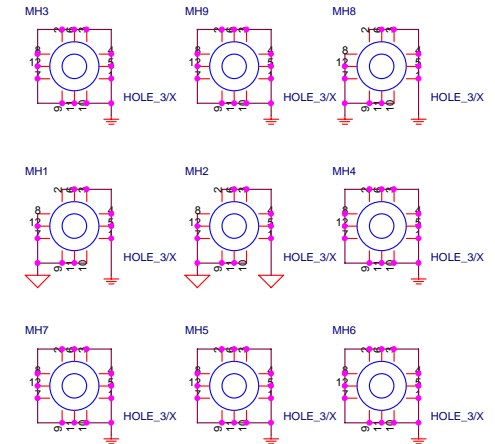


CPU-SK941AM3/S/GF/[10SC1-A01942-01R_10SC1-A01942-02R]

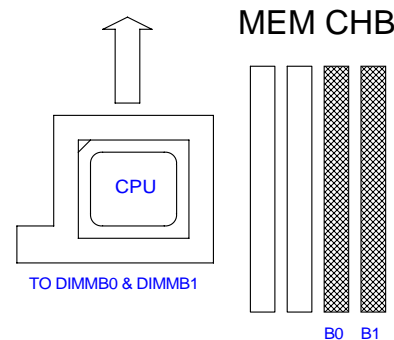
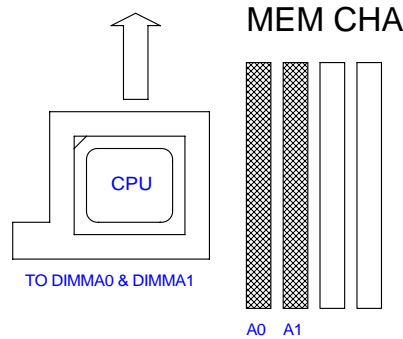
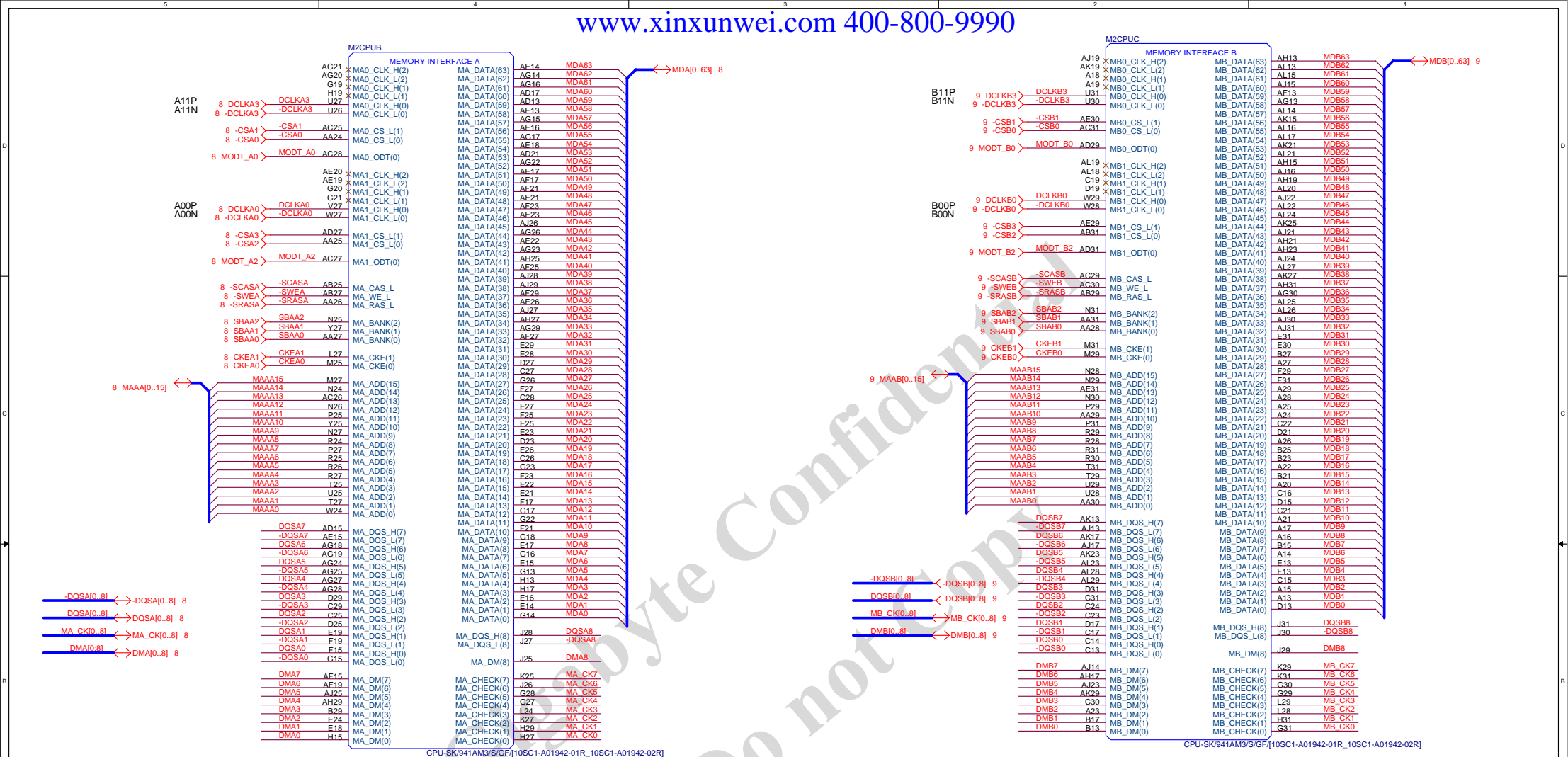


CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
 VLDT_B = HT12B



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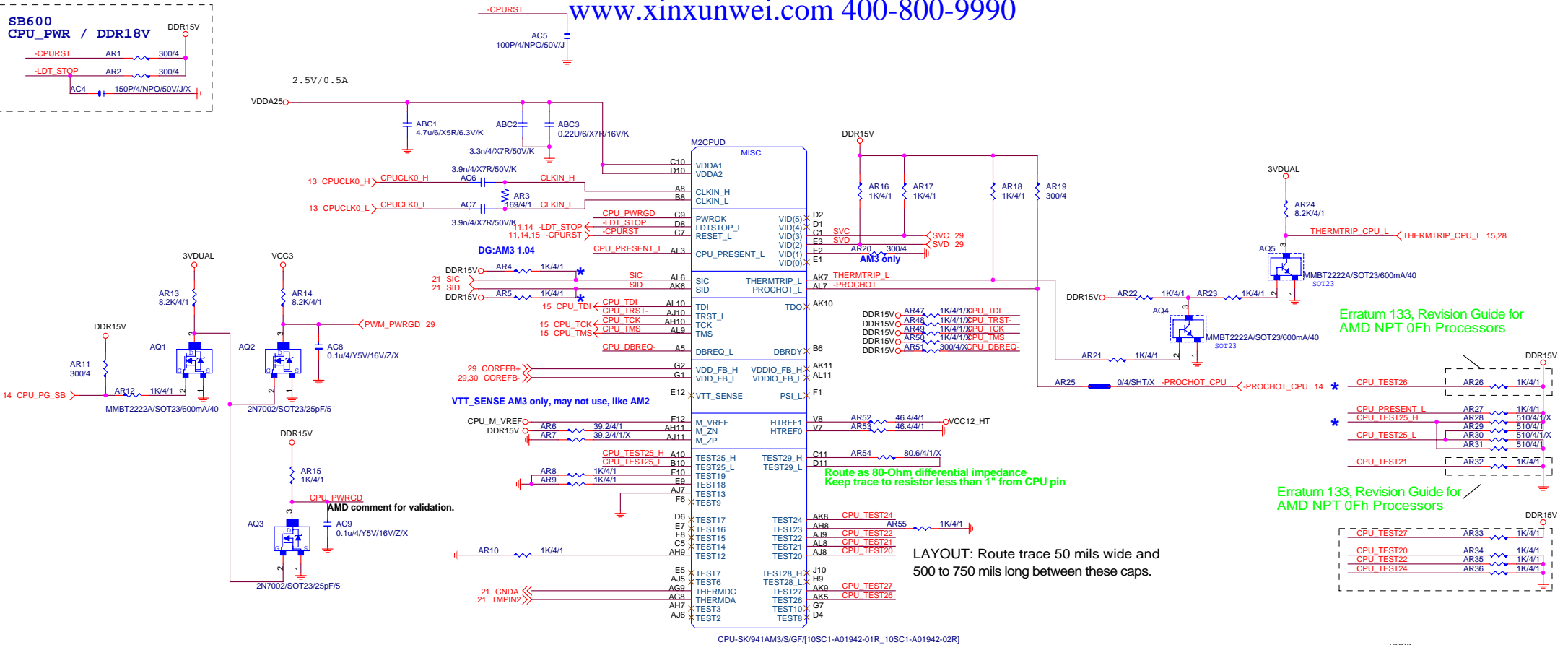
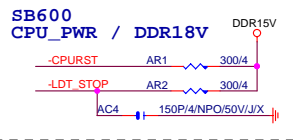


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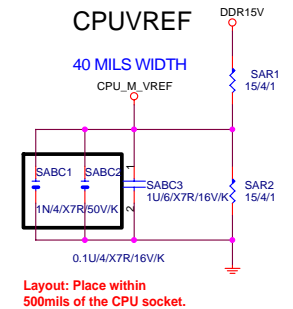
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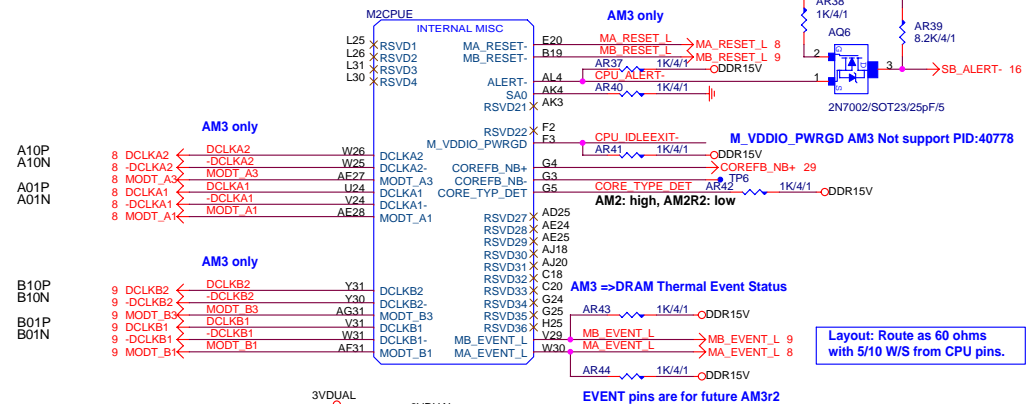
Erratum 133, Revision Guide for AMD NPT 0Fh Processors

Erratum 133, Revision Guide for AMD NPT 0Fh Processors

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.



Layout: Place within 500mils of the CPU socket.



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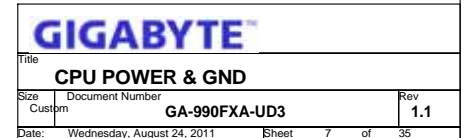
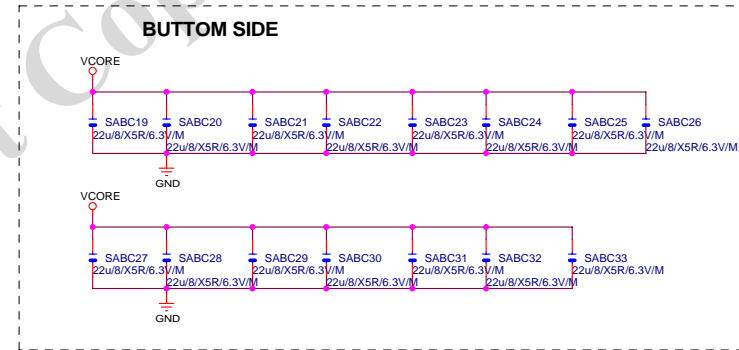
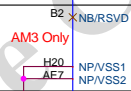
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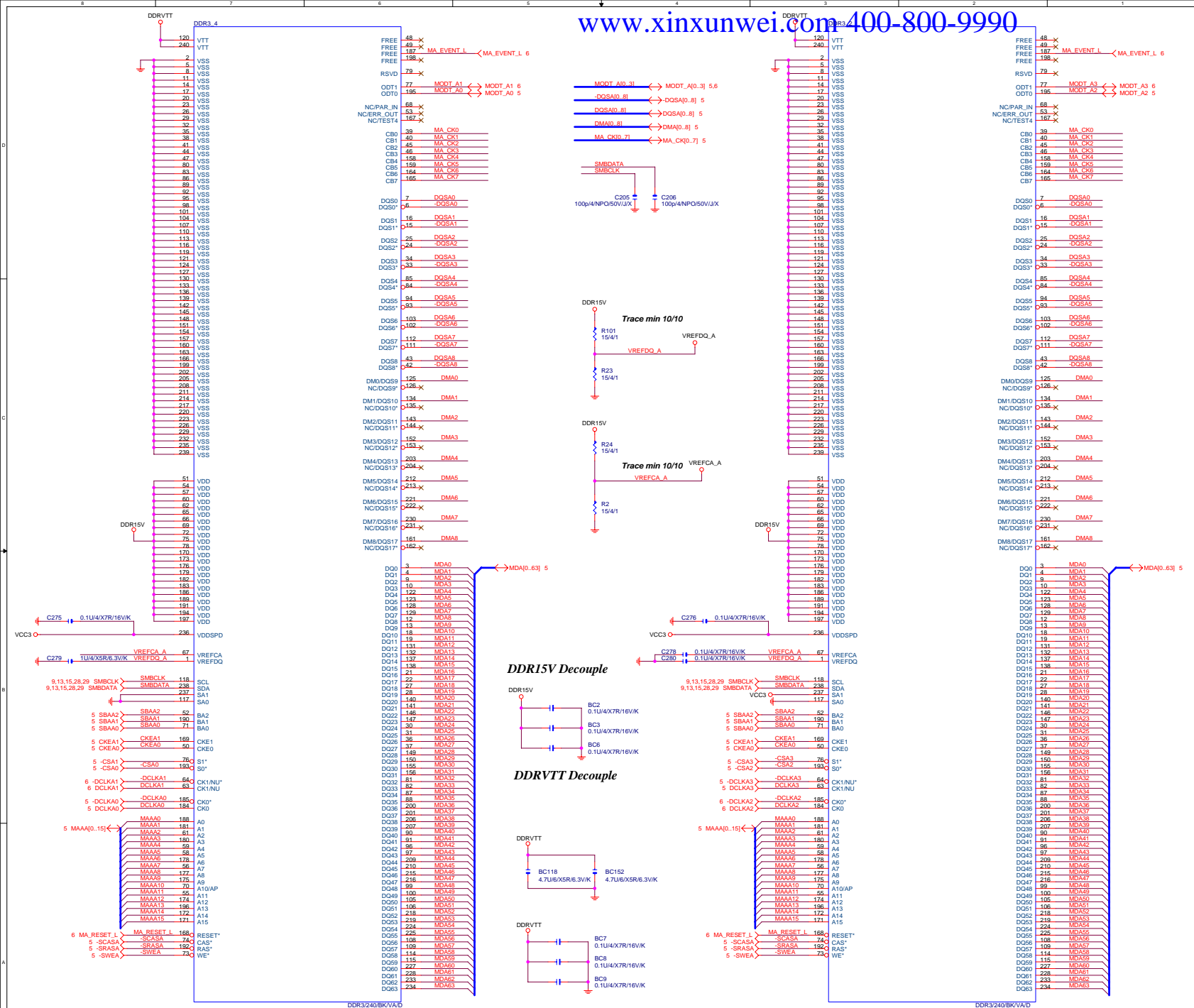
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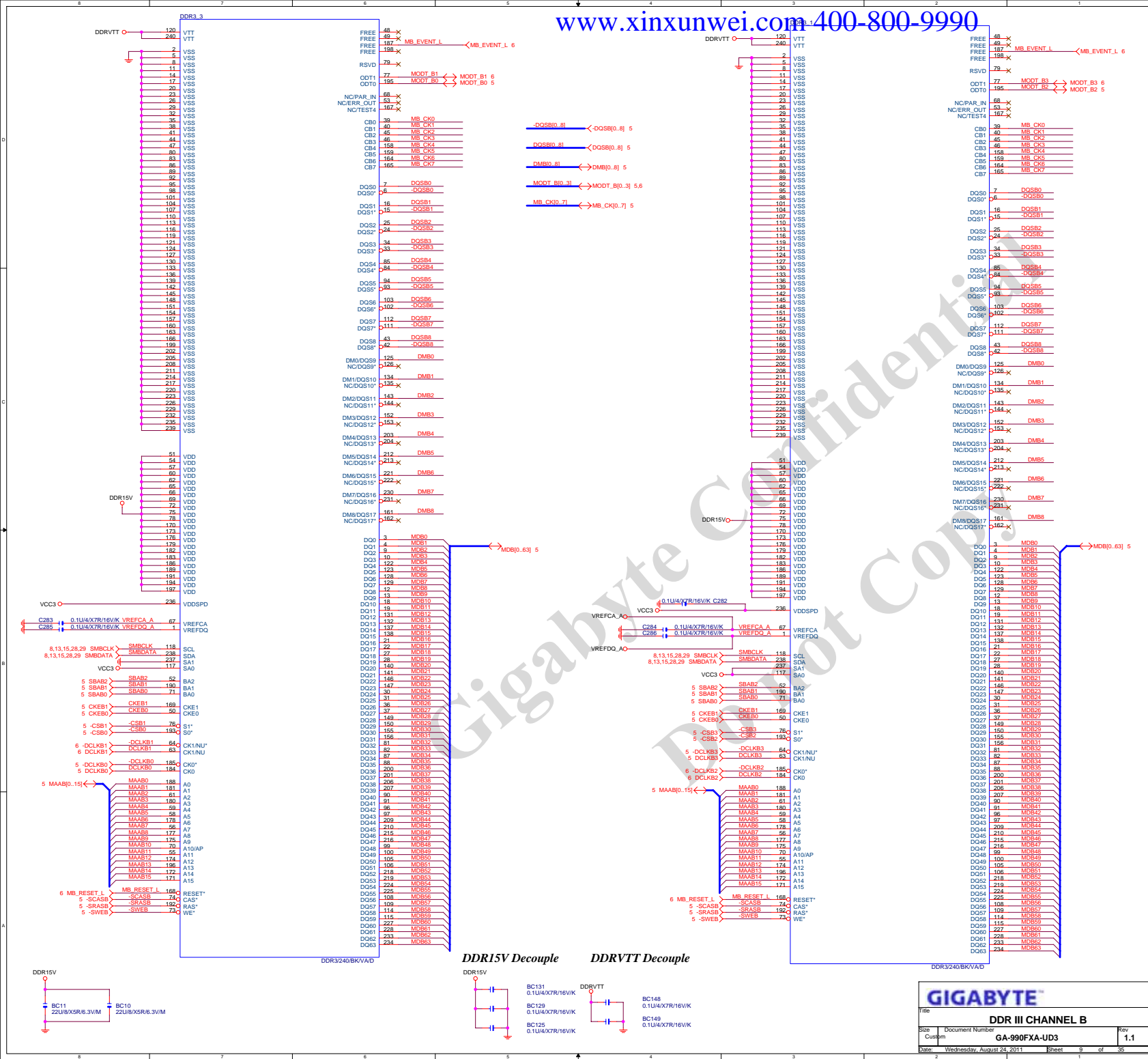
Customer

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U3A

PART 1/5

PART 2/5

HYPERTRANSPORT
IF

L0_CADOUT_H15	T25	HT_RXCAD15P	HT_TXCAD15P	N23	L0_CADIN_H15
L0_CADOUT_L15	T24	HT_RXCAD15N	HT_TXCAD15N	N24	L0_CADIN_L15
L0_CADOUT_H14	U23	HT_RXCAD14P	HT_TXCAD14P	M25	L0_CADIN_H14
L0_CADOUT_L14	U23	HT_RXCAD14N	HT_TXCAD14N	M24	L0_CADIN_L14
L0_CADOUT_H13	V25	HT_RXCAD13P	HT_TXCAD13P	L23	L0_CADIN_H13
L0_CADOUT_L13	V24	HT_RXCAD13N	HT_TXCAD13N	L24	L0_CADIN_L13
L0_CADOUT_H12	W24	HT_RXCAD12P	HT_TXCAD12P	K24	L0_CADIN_H12
L0_CADOUT_L12	W23	HT_RXCAD12N	HT_TXCAD12N	K25	L0_CADIN_L12
L0_CADOUT_H11	AA24	HT_RXCAD11P	HT_TXCAD11P	H24	L0_CADIN_H11
L0_CADOUT_L11	AA23	HT_RXCAD11N	HT_TXCAD11N	H25	L0_CADIN_L11
L0_CADOUT_H10	AB25	HT_RXCAD10P	HT_TXCAD10P	G23	L0_CADIN_H10
L0_CADOUT_L10	AB24	HT_RXCAD10N	HT_TXCAD10N	G24	L0_CADIN_L10
L0_CADOUT_H9	AC23	HT_RXCAD9P	HT_TXCAD9P	F24	L0_CADIN_H9
L0_CADOUT_L9	AC24	HT_RXCAD9N	HT_TXCAD9N	F25	L0_CADIN_L9
L0_CADOUT_H8	AD25	HT_RXCAD8P	HT_TXCAD8P	E23	L0_CADIN_H8
L0_CADOUT_L8	AD24	HT_RXCAD8N	HT_TXCAD8N	E24	L0_CADIN_L8
L0_CADOUT_H7	T27	HT_RXCAD7P	HT_TXCAD7P	N26	L0_CADIN_H7
L0_CADOUT_L7	T27	HT_RXCAD7N	HT_TXCAD7N	M27	L0_CADIN_L7
L0_CADOUT_H6	U27	HT_RXCAD6P	HT_TXCAD6P	M28	L0_CADIN_H6
L0_CADOUT_L6	U26	HT_RXCAD6N	HT_TXCAD6N	L26	L0_CADIN_L6
L0_CADOUT_H5	V28	HT_RXCAD5P	HT_TXCAD5P	L27	L0_CADIN_H5
L0_CADOUT_L5	V27	HT_RXCAD5N	HT_TXCAD5N	K27	L0_CADIN_L5
L0_CADOUT_H4	W27	HT_RXCAD4P	HT_TXCAD4P	K28	L0_CADIN_L4
L0_CADOUT_L4	W26	HT_RXCAD4N	HT_TXCAD4N	H27	L0_CADIN_H3
L0_CADOUT_H3	AA27	HT_RXCAD3P	HT_TXCAD3P	H28	L0_CADIN_L3
L0_CADOUT_L3	AA26	HT_RXCAD3N	HT_TXCAD3N	G26	L0_CADIN_H2
L0_CADOUT_H2	AB28	HT_RXCAD2P	HT_TXCAD2P	G27	L0_CADIN_L2
L0_CADOUT_L2	AB27	HT_RXCAD2N	HT_TXCAD2N	E27	L0_CADIN_H1
L0_CADOUT_H1	AC27	HT_RXCAD1P	HT_TXCAD1P	F28	L0_CADIN_L1
L0_CADOUT_L1	AC26	HT_RXCAD1N	HT_TXCAD1N	E28	L0_CADIN_H0
L0_CADOUT_H0	AD28	HT_RXCAD0P	HT_TXCAD0P	E29	L0_CADIN_L0
L0_CADOUT_L0	AD27	HT_RXCAD0N	HT_TXCAD0N		

4 L0_CLKOUT_H1	L0_CLKOUT_H1	Y25	HT_RXCLK1P	HT_TXCLK1P	J23	L0_CLKIN_H1	L0_CLKIN_H1	4
4 L0_CLKOUT_L1	L0_CLKOUT_L1	Y24	HT_RXCLK1N	HT_TXCLK1N	J24	L0_CLKIN_L1	L0_CLKIN_L1	4
4 L0_CLKOUT_H0	L0_CLKOUT_H0	Y28	HT_RXCLK0P	HT_TXCLK0P	J26	L0_CLKIN_H0	L0_CLKIN_L0	4
4 L0_CLKOUT_L0	L0_CLKOUT_L0	Y27	HT_RXCLK0N	HT_TXCLK0N	J27	L0_CLKIN_L0	L0_CLKIN_L0	4

4 L0_CTLOUT_H1	L0_CTLOUT_H1	R24	HT_RXCTL1P	HT_TXCTL1P	P24	L0_CTLIN_H1	L0_CTLIN_H1	4
4 L0_CTLOUT_L1	L0_CTLOUT_L1	R23	HT_RXCTL1N	HT_TXCTL1N	P25	L0_CTLIN_L1	L0_CTLIN_L1	4
4 L0_CTLOUT_H0	L0_CTLOUT_H0	R27	HT_RXCTL0P	HT_TXCTL0P	P27	L0_CTLIN_H0	L0_CTLIN_L0	4
4 L0_CTLOUT_L0	L0_CTLOUT_L0	R26	HT_RXCTL0N	HT_TXCTL0N	P28	L0_CTLIN_L0	L0_CTLIN_L0	4

SNR0	1.21K/4/1	HT_RXCALN	D25	HT_RXCALP	D24	HT_RXCALN	HT_TXCALN	NR1	1.21K/4/1
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L0_CADIN_H10_15I	L0_CADIN_H10_15I	4
L0_CADIN_L10_15I	L0_CADIN_L10_15I	4

4 L0_CADOUT_H10_15I	L0_CADOUT_H10_15I	
4 L0_CADOUT_L10_15I	L0_CADOUT_L10_15I	

EXP_A_RXP10_15I	EXP_A_RXP10_15I	18
EXP_A_RXN10_15I	EXP_A_RXN10_15I	18
EXP_A_TXP10_15I	EXP_A_TXP10_15I	18
EXP_A_TXN10_15I	EXP_A_TXN10_15I	18

EXP_B_TXP10_15I	EXP_B_TXP10_15I	19
EXP_B_TXN10_15I	EXP_B_TXN10_15I	19

EXP_B_RXP10_15I	EXP_B_RXP10_15I	19
EXP_B_RXN10_15I	EXP_B_RXN10_15I	19

20 PCIE4_4P	AD11	GP33_RX9P	GP33_RX9P	AD11	GP33_RX9P
20 PCIE4_4N	AD11	GP33_RX9N	GP33_RX9N	AD11	GP33_RX9N
20 PCIE4_3P	AE12	GP33_RX8P	GP33_RX8P	AD12	GP33_RX8P
20 PCIE4_3N	AD12	GP33_RX8N	GP33_RX8N	AD13	GP33_RX8N
20 PCIE4_2P	AD13	GP33_RX7P	GP33_RX7P	AD14	GP33_RX7P
20 PCIE4_2N	AD14	GP33_RX7N	GP33_RX7N	AD15	GP33_RX7N
20 PCIE4_1P	AE14	GP33_RX6P	GP33_RX6P	AD16	GP33_RX6P
20 PCIE4_1N	AD15	GP33_RX6N	GP33_RX6N	AD17	GP33_RX6N
32 RB_SL_IP	AD16	GP33_RX5P	GP33_RX5P	AD18	GP33_RX5P
33 UB_USB3_IP	AD17	GP33_RX5N	GP33_RX5N	AD19	GP33_RX5N
33 UB_USB3_SB	AD18	GP33_RX4P	GP33_RX4P	AD20	GP33_RX4P
19 PCIE4_4P_SB	AD19	GP33_RX4N	GP33_RX4N	AD21	GP33_RX4N
19 PCIE4_4N_SB	AD20	GP33_RX3P	GP33_RX3P	AD22	GP33_RX3P
19 PCIE4_3P_SB	AD21	GP33_RX3N	GP33_RX3N	AD23	GP33_RX3N
19 PCIE4_3N_SB	AD22	GP33_RX2P	GP33_RX2P	AD24	GP33_RX2P
19 PCIE4_2P_SB	AD23	GP33_RX2N	GP33_RX2N	AD25	GP33_RX2N
19 PCIE4_2N_SB	AD24	GP33_RX1P	GP33_RX1P	AD26	GP33_RX1P
19 PCIE4_1P_SB	AD25	GP33_RX1N	GP33_RX1N	AD27	GP33_RX1N
19 PCIE4_1N_SB	AD26	GP33_RX0P	GP33_RX0P	AD28	GP33_RX0P
	AG20	GP33_RX0N	GP33_RX0N	AG20	GP33_RX0N

14 A_RX3P	AC21	SB_RX3P	SB_RX3P	AC21	SB_RX3P
14 A_RX3N	AD21	SB_RX3N	SB_RX3N	AD21	SB_RX3N
14 A_RX2P	AE22	SB_RX2P	SB_RX2P	AE22	SB_RX2P
14 A_RX2N	AG25	SB_RX2N	SB_RX2N	AG25	SB_RX2N
14 A_RX1P	AG26	SB_RX1P	SB_RX1P	AG26	SB_RX1P
14 A_RX1N	AG26	SB_RX1N	SB_RX1N	AG26	SB_RX1N
14 A_RX0P	AG26	SB_RX0P	SB_RX0P	AG26	SB_RX0P
14 A_RX0N	AG26	SB_RX0N	SB_RX0N	AG26	SB_RX0N

SB_TX3P	AG22	A_TX3P	A_TX3P	AG22	A_TX3P
SB_TX3N	AG22	A_TX3N	A_TX3N	AG22	A_TX3N
SB_TX2P	AG21	A_TX2P	A_TX2P	AG21	A_TX2P
SB_TX2N	AG21	A_TX2N	A_TX2N	AG21	A_TX2N
SB_TX1P	AG23	A_TX1P	A_TX1P	AG23	A_TX1P
SB_TX1N	AG23	A_TX1N	A_TX1N	AG23	A_TX1N
SB_TX0P	AG24	A_TX0P	A_TX0P	AG24	A_TX0P
SB_TX0N	AG24	A_TX0N	A_TX0N	AG24	A_TX0N

PCIE_BCALRP	PCIE_BCALRP	PCIE_BCALRP	PCIE_BCALRP	PCIE_BCALRP	PCIE_BCALRP
PCIE_RCALRP	PCIE_RCALRP	PCIE_RCALRP	PCIE_RCALRP	PCIE_RCALRP	PCIE_RCALRP
PCIE_TCALRP	PCIE_TCALRP	PCIE_TCALRP	PCIE_TCALRP	PCIE_TCALRP	PCIE_TCALRP

PCIE_ALINK	PCIE_ALINK	PCIE_ALINK	PCIE_ALINK	PCIE_ALINK	PCIE_ALINK
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PCIE_GPP2	PCIE_GPP2	PCIE_GPP2	PCIE_GPP2	PCIE_GPP2	PCIE_GPP2
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PCIE_GPP5	PCIE_GPP5	PCIE_GPP5	PCIE_GPP5	PCIE_GPP5	PCIE_GPP5
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PCIE_GPP6	PCIE_GPP6	PCIE_GPP6	PCIE_GPP6	PCIE_GPP6	PCIE_GPP6
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PCIE_GPP7	PCIE_GPP7	PCIE_GPP7	PCIE_GPP7	PCIE_GPP7	PCIE_GPP7
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PCIE_GPP8	PCIE_GPP8	PCIE_GPP8	PCIE_GPP8	PCIE_GPP8	PCIE_GPP8
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PCIE_GPP9	PCIE_GPP9	PCIE_GPP9	PCIE_GPP9	PCIE_GPP9	PCIE_GPP9
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PCIE_GPP10	PCIE_GPP10	PCIE_GPP10	PCIE_GPP10	PCIE_GPP10	PCIE_GPP10
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PCIE_GPP11	PCIE_GPP11	PCIE_GPP11	PCIE_GPP11	PCIE_GPP11	PCIE_GPP11
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PCIE_GPP12	PCIE_GPP12	PCIE_GPP12	PCIE_GPP12	PCIE_GPP12	PCIE_GPP12
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PCIE_GPP13	PCIE_GPP13	PCIE_GPP13	PCIE_GPP13	PCIE_GPP13	PCIE_GPP13
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PCIE_GPP14	PCIE_GPP14	PCIE_GPP14	PCIE_GPP14	PCIE_GPP14	PCIE_GPP14
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PCIE_GPP15	PCIE_GPP15	PCIE_GPP15	PCIE_GPP15	PCIE_GPP15	PCIE_GPP15
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PCIE_GPP16	PCIE_GPP16	PCIE_GPP16	PCIE_GPP16	PCIE_GPP16	PCIE_GPP16
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PCIE_GPP17	PCIE_GPP17	PCIE_GPP17	PCIE_GPP17	PCIE_GPP17	PCIE_GPP17
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PCIE_GPP23	PCIE_GPP23	PCIE_GPP23	PCIE_GPP23	PCIE_GPP23	PCIE_GPP23
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PCIE_GPP24	PCIE_GPP24	PCIE_GPP24	PCIE_GPP24	PCIE_GPP24	PCIE_GPP24
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PCIE_GPP25	PCIE_GPP25	PCIE_GPP25	PCIE_GPP25	PCIE_GPP25	PCIE_GPP25
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PCIE_GPP26	PCIE_GPP26	PCIE_GPP26	PCIE_GPP26	PCIE_GPP26	PCIE_GPP26
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PCIE_GPP27	PCIE_GPP27	PCIE_GPP27	PCIE_GPP27	PCIE_GPP27	PCIE_GPP27
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PCIE_GPP30	PCIE_GPP30	PCIE_GPP30	PCIE_GPP30	PCIE_GPP30	PCIE_GPP30
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PCIE_GPP31	PCIE_GPP31	PCIE_GPP31	PCIE_GPP31	PCIE_GPP31	PCIE_GPP31
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PCIE_GPP33	PCIE_GPP33	PCIE_GPP33	PCIE_GPP33	PCIE_GPP33	PCIE_GPP33
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PCIE_GPP34	PCIE_GPP34	PCIE_GPP34	PCIE_GPP34	PCIE_GPP34	PCIE_GPP34
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PCIE_GPP35	PCIE_GPP35	PCIE_GPP35	PCIE_GPP35	PCIE_GPP35	PCIE_GPP35
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PCIE_GPP36	PCIE_GPP36	PCIE_GPP36	PCIE_GPP36	PCIE_GPP36	PCIE_GPP36
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PCIE_GPP37	PCIE_GPP37	PCIE_GPP37	PCIE_GPP37	PCIE_GPP37	PCIE_GPP37
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PCIE_GPP38	PCIE_GPP38	PCIE_GPP38	PCIE_GPP38	PCIE_GPP38	PCIE_GPP38
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PCIE_GPP44	PCIE_GPP44	PCIE_GPP44	PCIE_GPP44	PCIE_GPP44	PCIE_GPP44
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PCIE_GPP45	PCIE_GPP45	PCIE_GPP45	PCIE_GPP45	PCIE_GPP45	PCIE_GPP45
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PCIE_GPP46	PCIE_GPP46	PCIE_GPP46	PCIE_GPP46	PCIE_GPP46	PCIE_GPP46
------------	------------	------------	------------	------------	------------

PCIE_GPP47	PCIE_GPP47	PCIE_GPP47	PCIE_GPP47	PCIE_GPP47	PCIE_GPP47
------------	------------	------------	------------	------------	------------

PCIE_GPP48	PCIE_GPP48	PCIE_GPP48	PCIE_GPP48	PCIE_GPP48	PCIE_GPP48
------------	------------	------------	------------	------------	------------

PCIE_GPP49	PCIE_GPP49	PCIE_GPP49	PCIE_GPP49	PCIE_GPP49	PCIE_GPP49
------------	------------	------------	------------	------------	------------

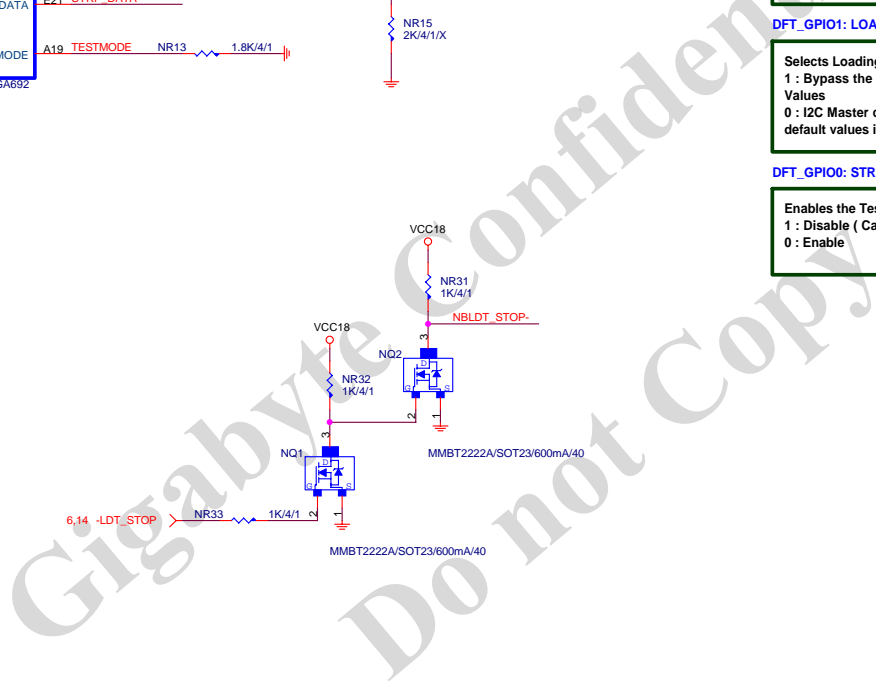
PCIE_GPP50	PCIE_GPP50	PCIE_GPP50	PCIE_GPP50	PCIE_GPP50	PCIE_GPP50
------------	------------	------------	------------	------------	------------

PCIE_GPP51	PCIE_GPP51	PCIE_GPP51	PCIE_GPP51	PCIE_GPP51	PCIE_GPP51
------------	------------	------------	------------	------------	------------

PCIE_GPP52	PCIE_GPP52	PCIE_GPP52	PCIE_GPP52	PCIE_GPP52	PCIE_GPP52
------------	------------	------------	------------	------------	------------

PCIE_GPP53	PCIE_GPP53	PCIE_GPP53	PCIE_GPP53	PCIE_GPP53	PCIE_GPP53
------------	------------	------------	------------	------------	------------

PCIE_GPP54	PCIE_GPP54	PCIE_GPP54	PCIE_GPP54	PCIE_GPP54	PCIE_GPP54
------------	------------	------------	------------	------------	------------

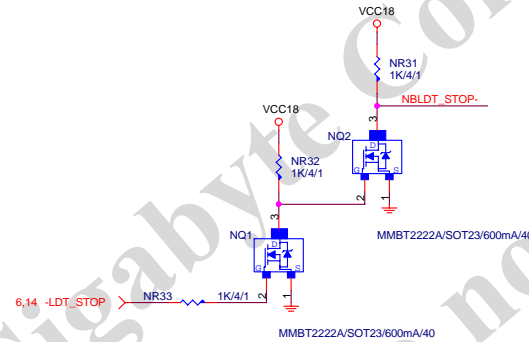


Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using
nbcfg register access)
0 : Enable

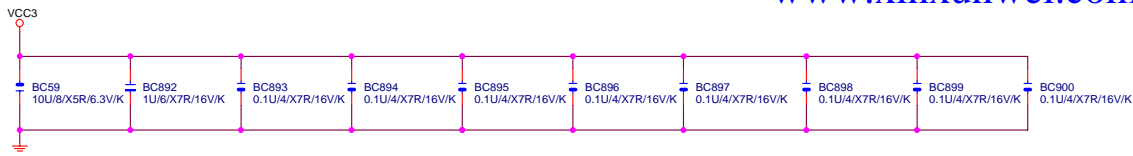
These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Enables the Test Debug Bus using PCIe bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable



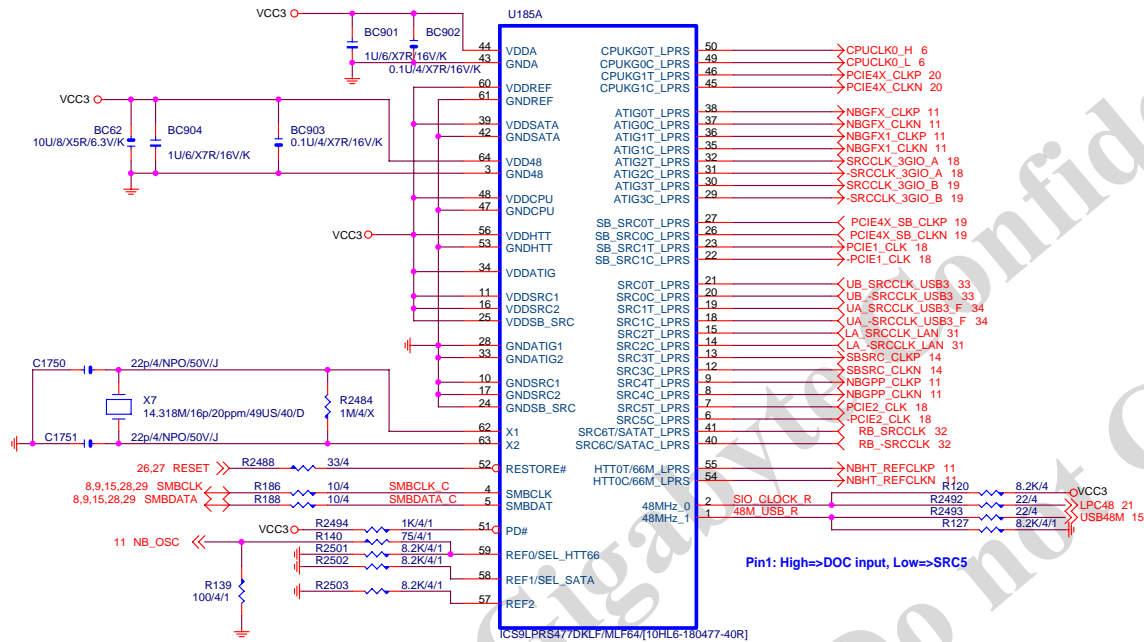




NB CLOCK INPUT TABLE

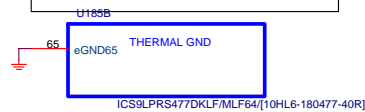
NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

* the GFX_REFCLK input is required for all cases



Pin1: High=>DOC input, Low=>SRC5

Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

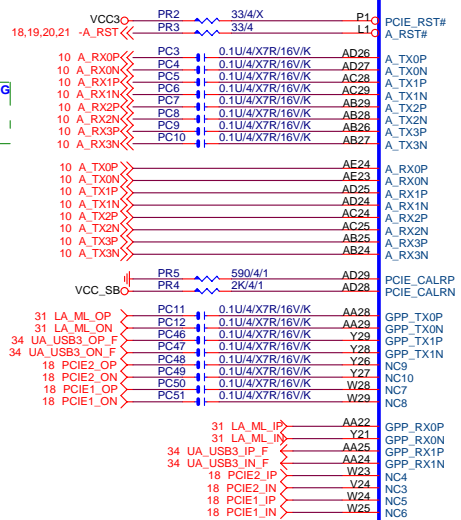
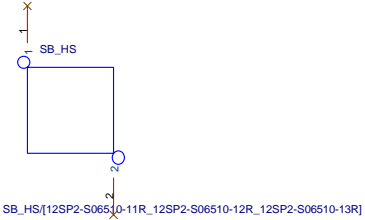
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK



PLACE THESE PCIE AC COUPLING CAPS CLOSE TO SB850

S.B HEATSINK



PCI EXPRESS INTERFACES

PCI INTERFACE

CLOCK GENERATOR

LPC

CPU

RTC

INTRUDER ALERT

VDDBT_RTC_G

SB950/BGA605

14M_25M_48M_OSC

25MHZ_X1

25MHZ_X2

25MHZ_X3

25MHZ_X4

25MHZ_X5

25MHZ_X6

25MHZ_X7

25MHZ_X8

25MHZ_X9

25MHZ_X10

25MHZ_X11

25MHZ_X12

25MHZ_X13

25MHZ_X14

25MHZ_X15

25MHZ_X16

25MHZ_X17

25MHZ_X18

25MHZ_X19

25MHZ_X20

25MHZ_X21

25MHZ_X22

25MHZ_X23

25MHZ_X24

25MHZ_X25

25MHZ_X26

25MHZ_X27

25MHZ_X28

25MHZ_X29

25MHZ_X30

25MHZ_X31

25MHZ_X32

25MHZ_X33

25MHZ_X34

25MHZ_X35

25MHZ_X36

25MHZ_X37

25MHZ_X38

25MHZ_X39

25MHZ_X40

25MHZ_X41

25MHZ_X42

25MHZ_X43

25MHZ_X44

25MHZ_X45

25MHZ_X46

25MHZ_X47

25MHZ_X48

25MHZ_X49

25MHZ_X50

25MHZ_X51

25MHZ_X52

25MHZ_X53

25MHZ_X54

25MHZ_X55

25MHZ_X56

25MHZ_X57

25MHZ_X58

25MHZ_X59

25MHZ_X60

25MHZ_X61

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25MHZ_X94

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25MHZ_X97

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25MHZ_X100

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25MHZ_X105

25MHZ_X106

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25MHZ_X109

25MHZ_X110

25MHZ_X111

25MHZ_X112

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25MHZ_X155

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25MHZ_X158

25MHZ_X159

25MHZ_X160

25MHZ_X161

25MHZ_X162

25MHZ_X163

25MHZ_X164

25MHZ_X165

25MHZ_X166

25MHZ_X167

25MHZ_X168

25MHZ_X169

25MHZ_X170

25MHZ_X171

25MHZ_X172

25MHZ_X173

25MHZ_X174

25MHZ_X175

25MHZ_X176

25MHZ_X177

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25MHZ_X190

25MHZ_X191

25MHZ_X192

25MHZ_X193

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25MHZ_X196

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25MHZ_X206

25MHZ_X207

25MHZ_X208

25MHZ_X209

25MHZ_X210

25MHZ_X211

25MHZ_X212

25MHZ_X213

25MHZ_X214

25MHZ_X215

25MHZ_X216

25MHZ_X217

25MHZ_X218

25MHZ_X219

25MHZ_X220

25MHZ_X221

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25MHZ_X225

25MHZ_X226

25MHZ_X227

25MHZ_X228

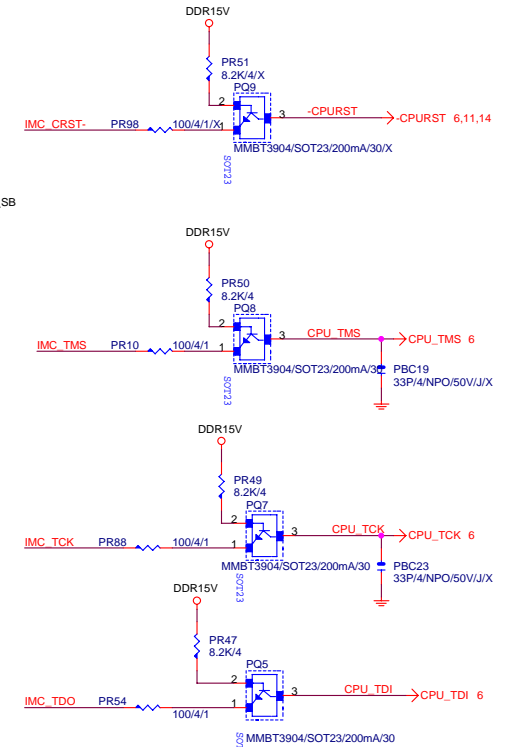
25MHZ_X229

25MHZ_X230

USB11 FRONT PANEL
 USB10 FRONT PANEL
 USB9 FRONT PANEL
 USB8 FRONT PANEL
 USB7 FRONT PANEL
 USB6 FRONT PANEL
 USB5 FRONT PANEL
 USB4 FRONT PANEL
 USB3 REAR PANEL
 USB2 REAR PANEL
 USB1 REAR PANEL
 USB0 REAR PANEL

either HWM inputs or PWR_GD signals
 can be used for power-up sequencer

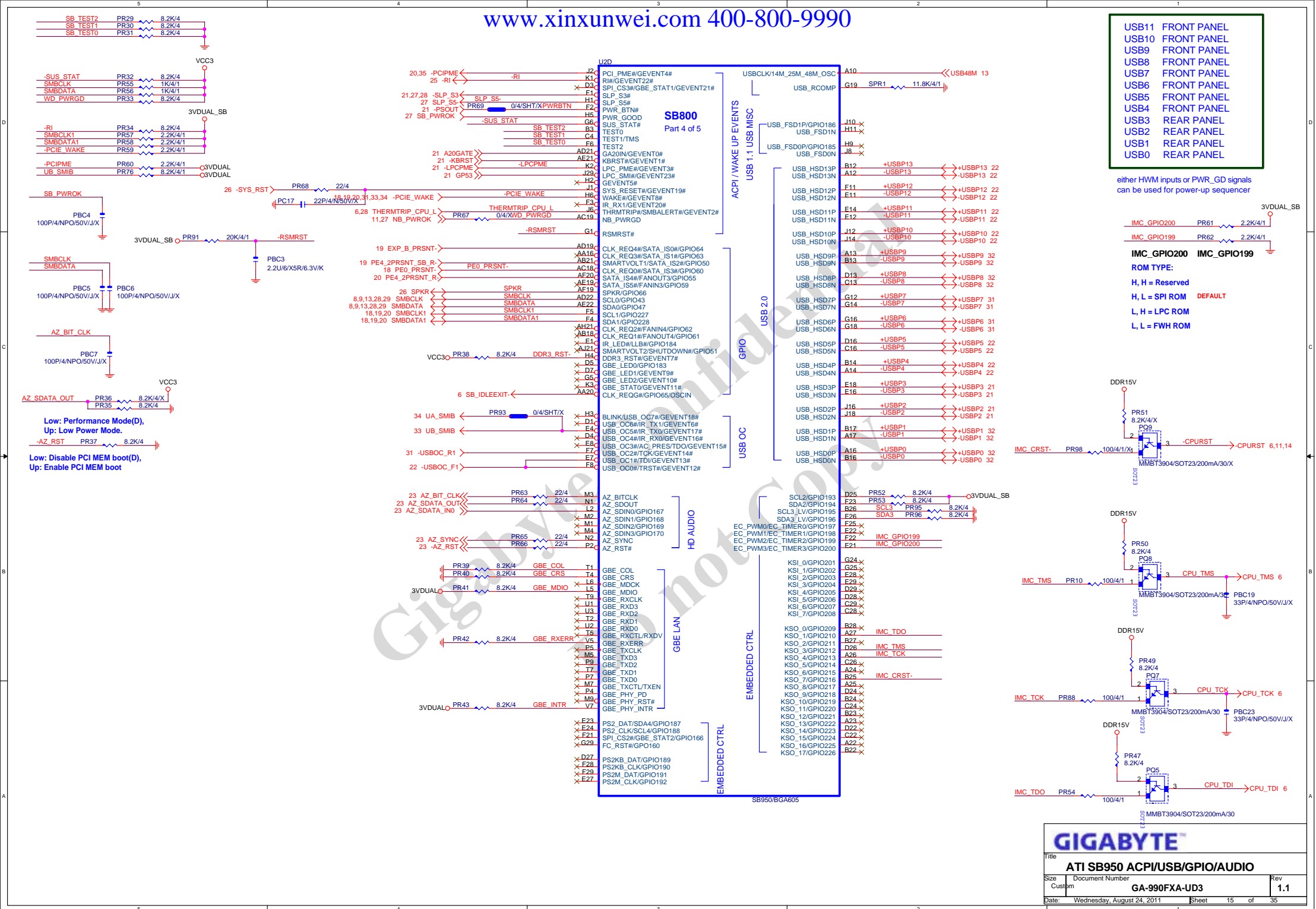
IMC_GPIO200 PR61 2.2K/4/1
 IMC_GPIO199 PR62 2.2K/4/1
IMC_GPIO200 IMC_GPIO199
ROM TYPE:
 H, H = Reserved
 L, L = SPI ROM **DEFAULT**
 L, H = LPC ROM
 L, L = FWH ROM



GIGABYTE

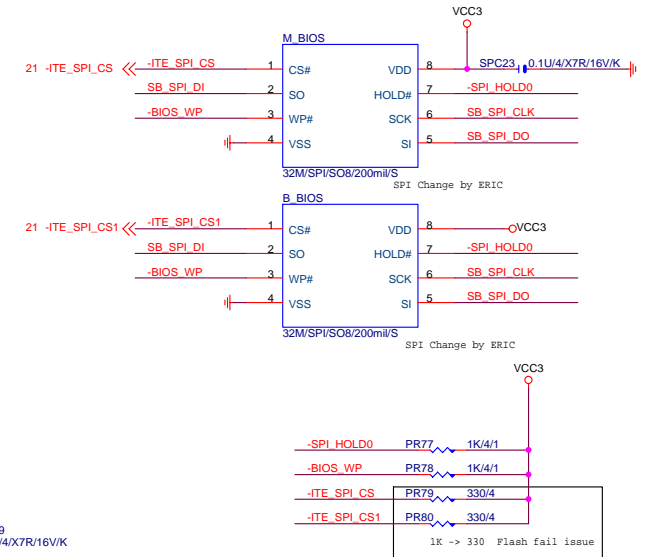
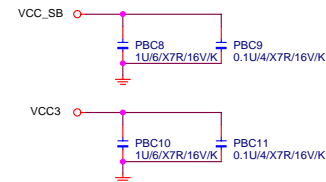
ATI SB950 ACPI/USB/GPIO/AUDIO

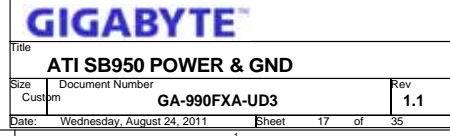
Size Document Number
 Custom GA-990FXA-UD3
 Date: Wednesday, August 24, 2011 Sheet 15 of 35





NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

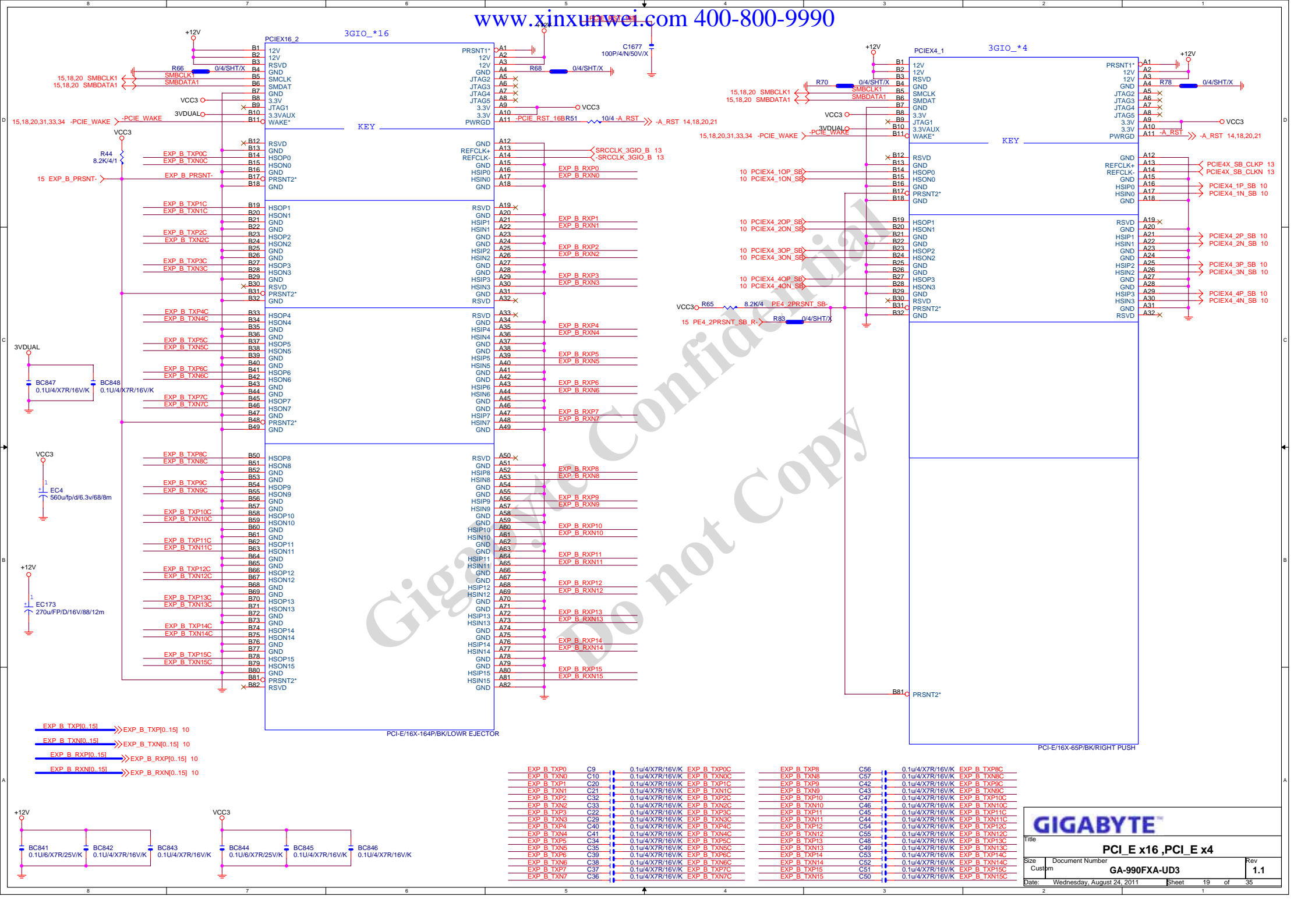


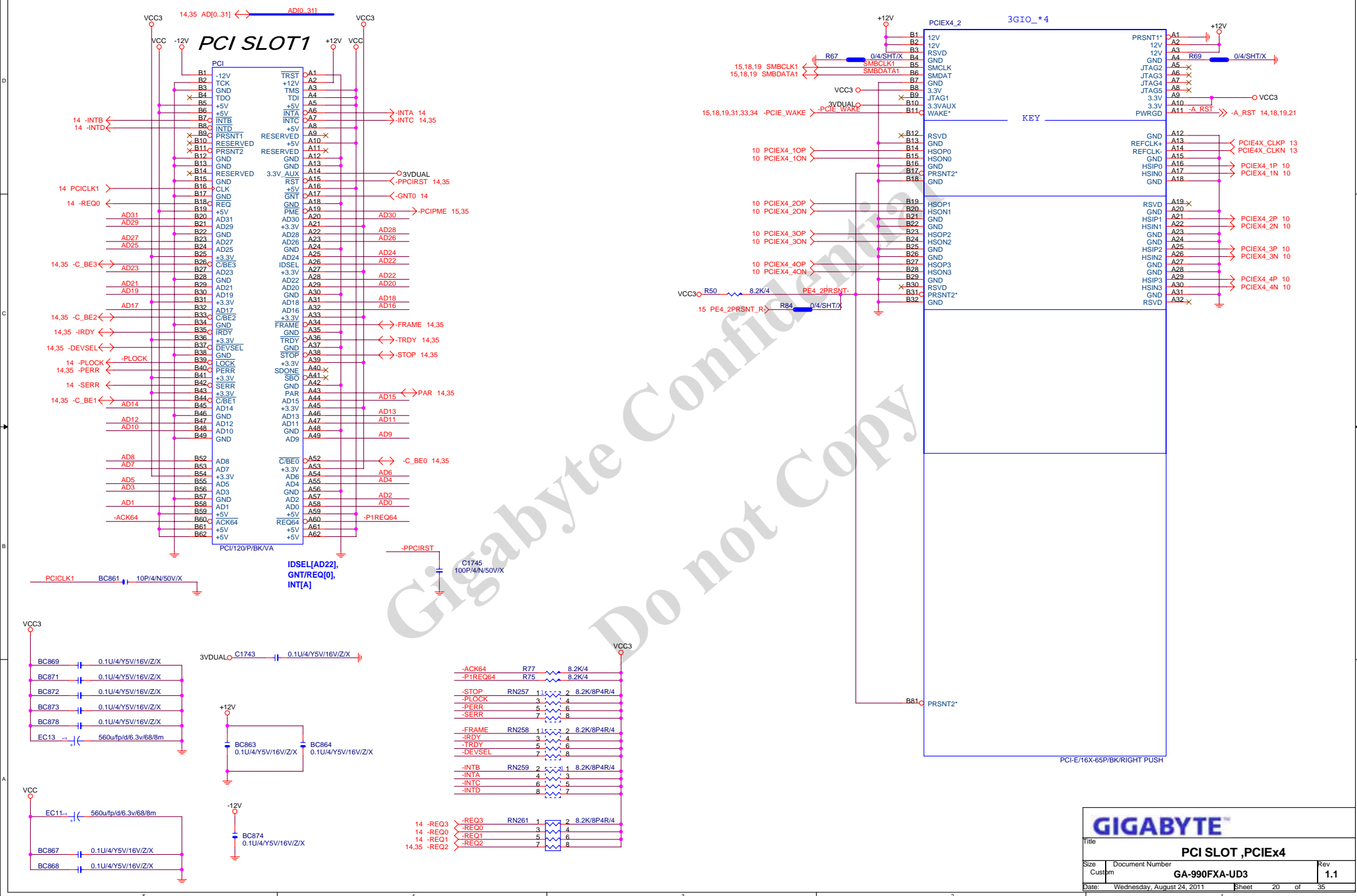




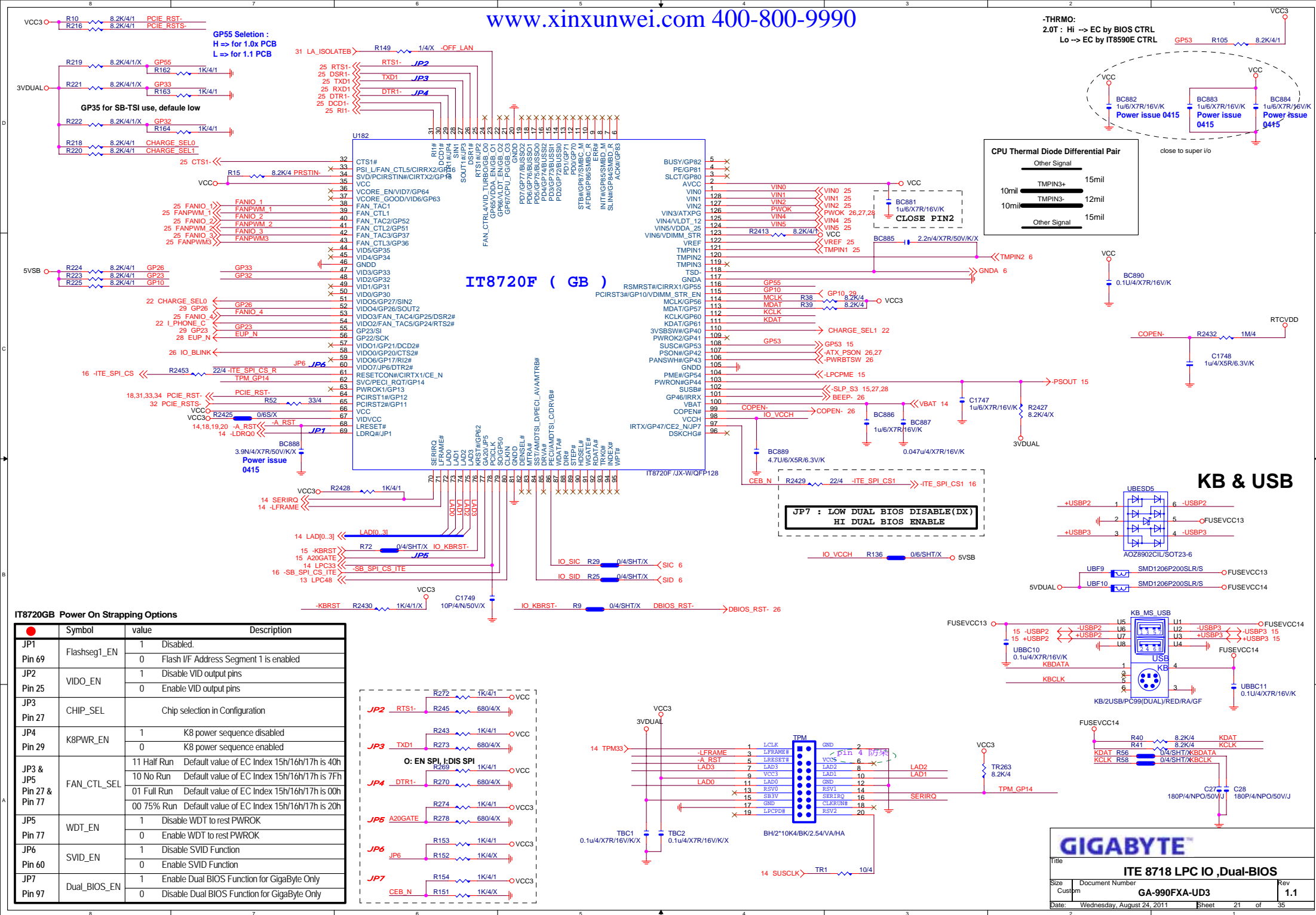
Size	Document Number
Custom	GA-990FXA-UD3

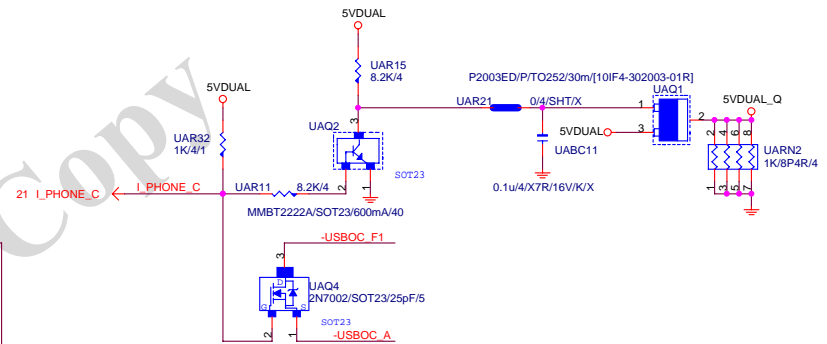
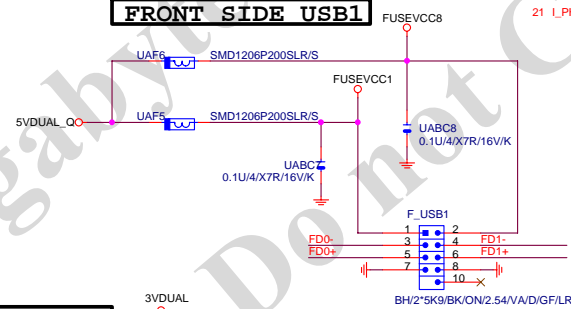
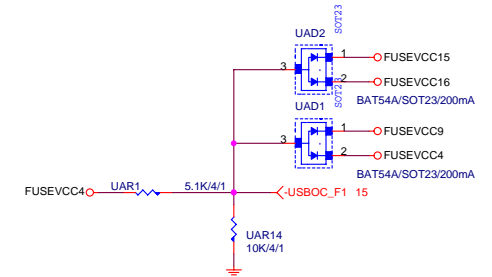
Date: Wednesday, August 24, 2011 Sheet 18 of 35



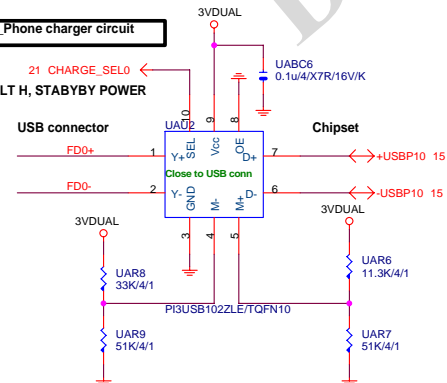


-THERMO:
2.0T : HI --> EC by BIOS CTRL
Lo --> EC by IT8590E CTRL

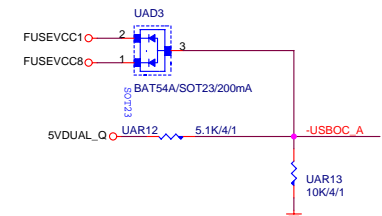
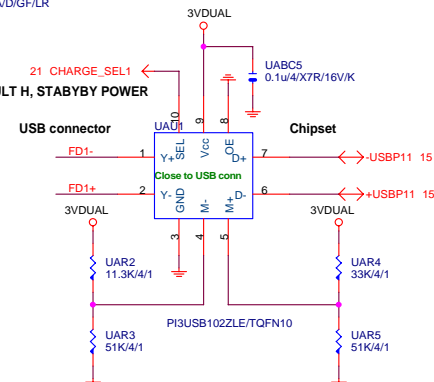




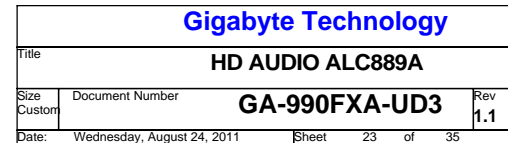
21 CHARGE_SEL0
DEFAULT H, STABYBY POWER



21 CHARGE_SEL1 ←
DEFAULT H, STABYBY POWER



62 ohm	
--------	--



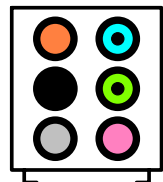
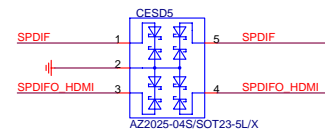
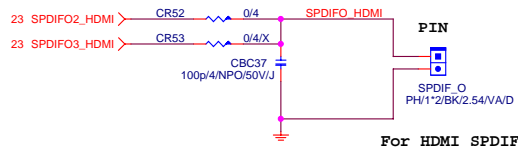
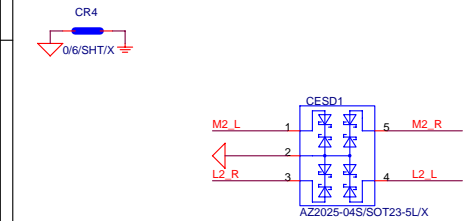
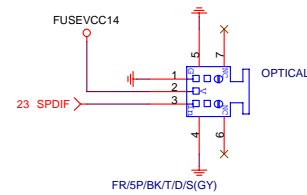
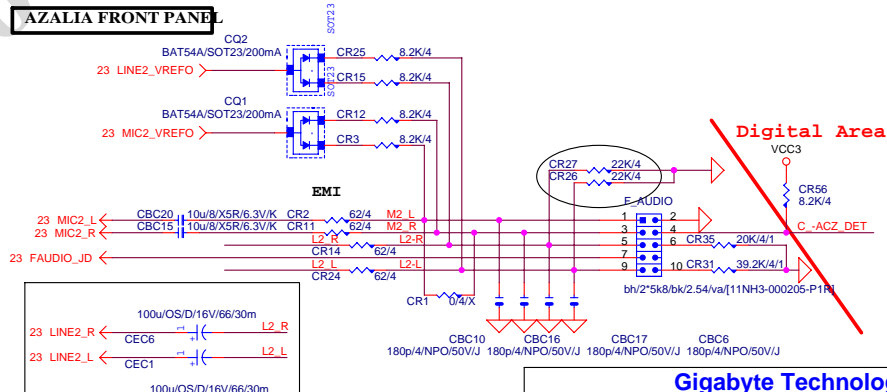
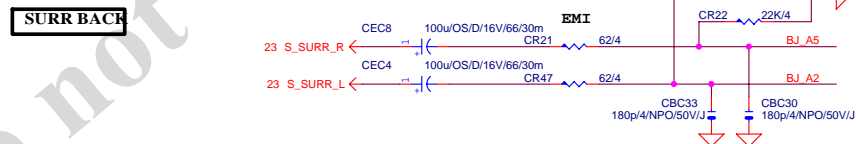
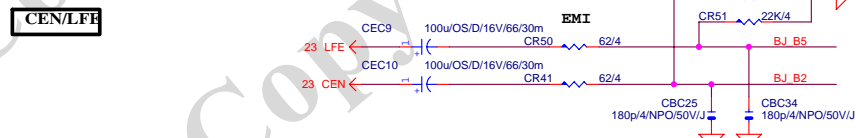
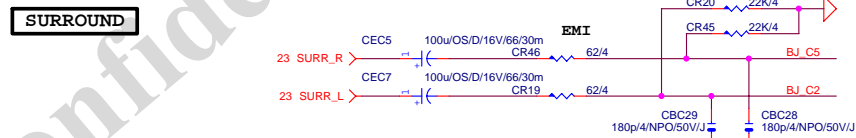
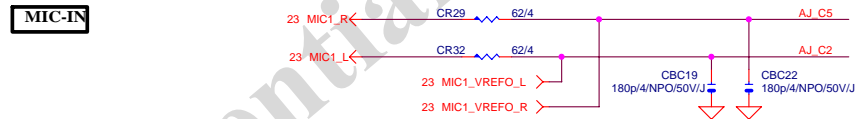
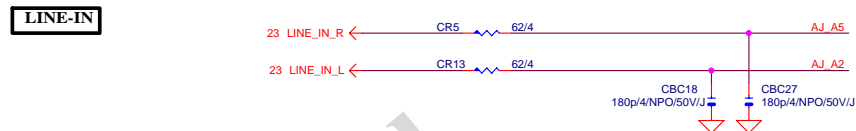
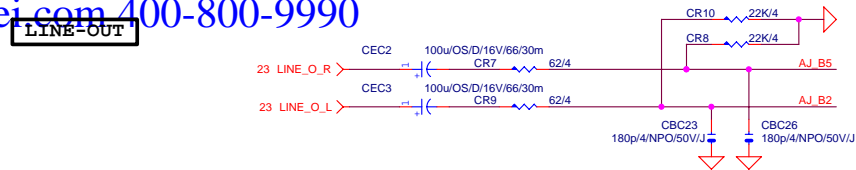
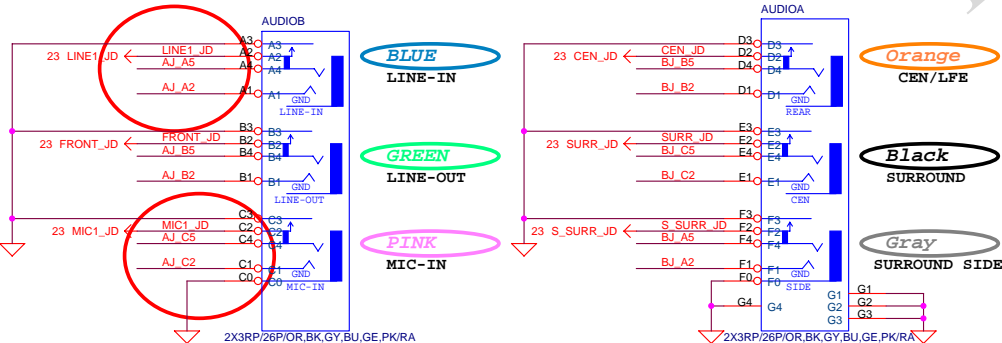


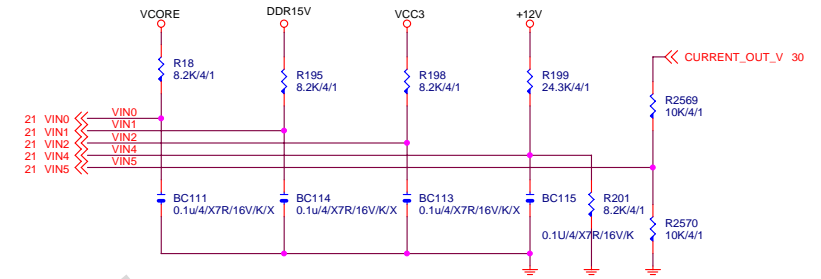
Diagram 1: CESD2. Connections: Pin 1 to AJ_A2, Pin 2 to AJ_C2, Pin 3 to AJ_B2, Pin 4 to AJ_C5. Ground symbol is connected to all pins.

Diagram 2: CESD4. Connections: Pin 1 to AJ_B5, Pin 2 to AJ_C2, Pin 4 to BJ_A2, Pin 5 to AJ_A5. Ground symbol is connected to all pins.

Diagram 3: CESD3. Connections: Pin 1 to BJ_B5, Pin 2 to BJ_C5, Pin 4 to BJ_A2, Pin 5 to BJ_A5. Ground symbol is connected to all pins.



Gigabyte Technology			
Title			
AUDIO JACK			
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DAU1

21 RH1 19 RY1 2 NR1A
 21 CT51 18 RY2 3 NC1SA
 21 DSR1 17 RY3 4 ND1SA
 21 RT31 16 DA1 5 NR1SA
 21 DTR1 15 DA2 6 ND1RA
 21 RXD1 14 RY4 7 NS1NA
 21 TXD1 13 DA3 8 NS1UTA
 21 DCD1 12 RY5 9 NC1DA

11 GND 20 VCC
 10 -12V 12V

0.1uF/4X7R/16V/K/X

GD75232/TSSOP20

0.1uF/4X7R/16V/K/X

0.1uF/4X7R/16V/K/X

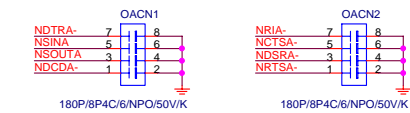
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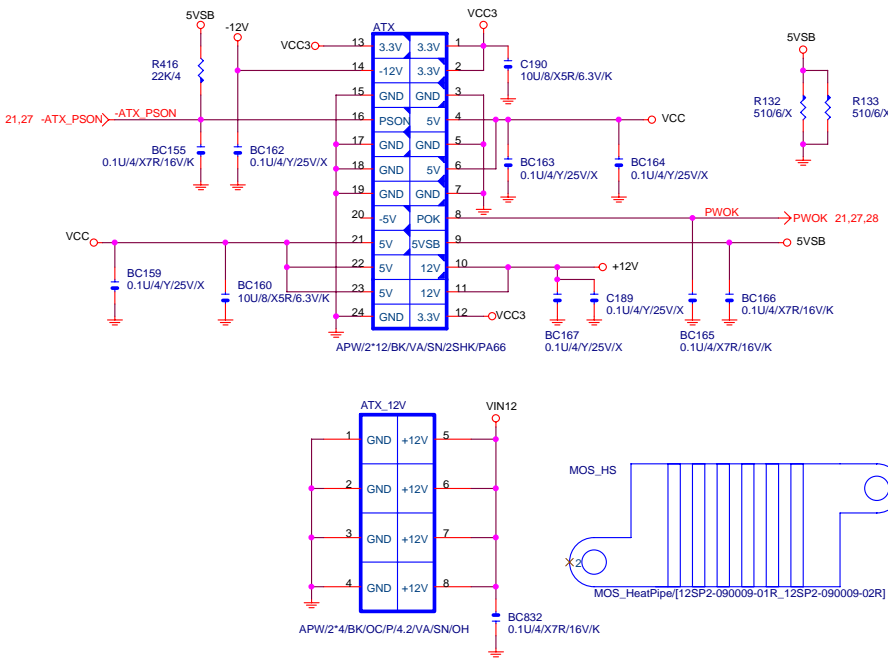
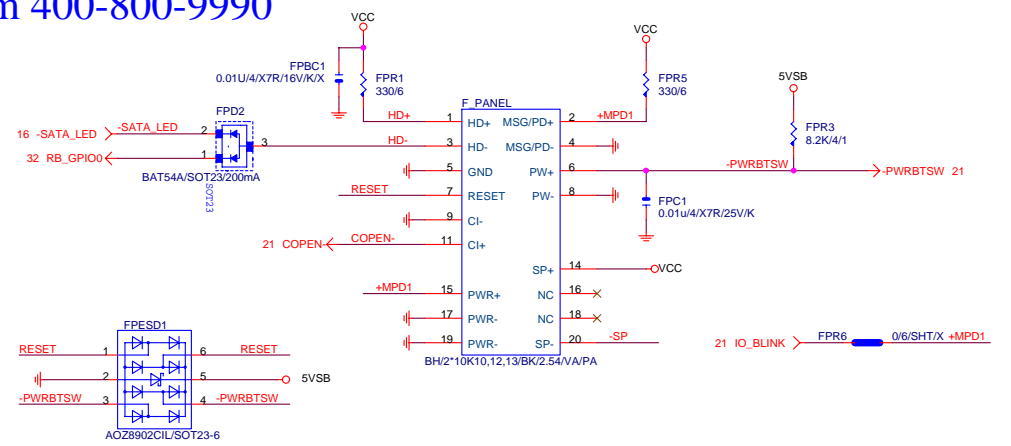
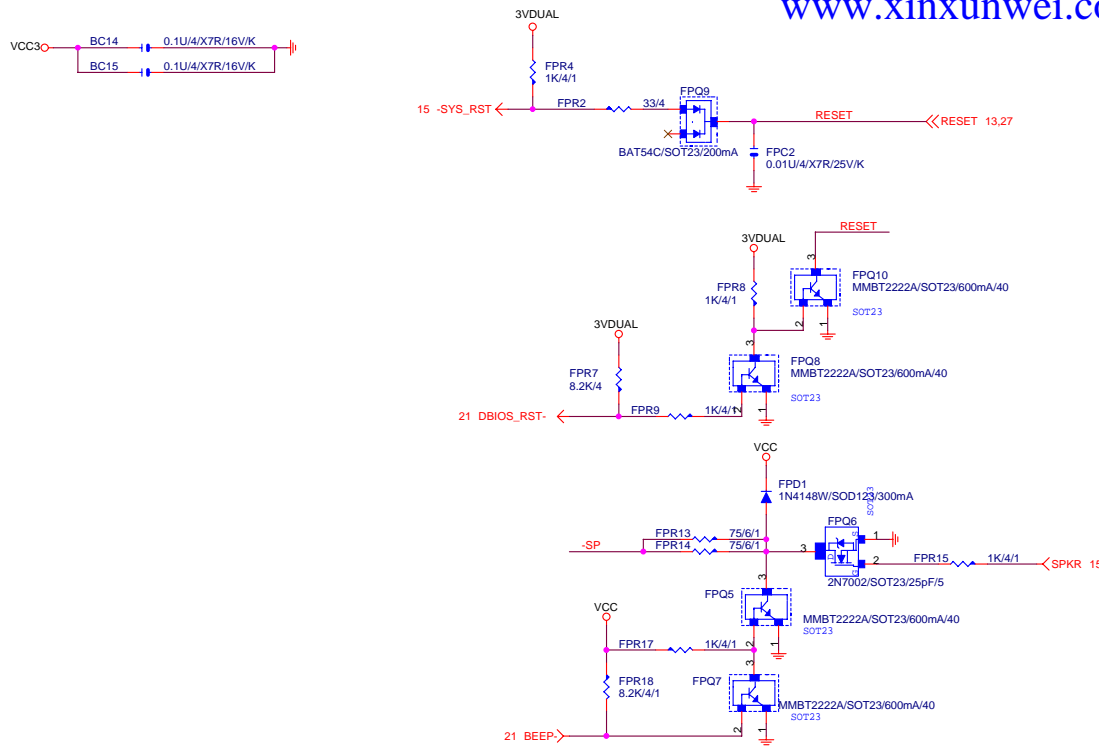
NDCDA-	1	2	NSINA
NSOUTA	3	4	NDTRA-
NRTSA-	5	6	NDSRA-
	7	8	NCTSA-
NRIA-	9	10	✕

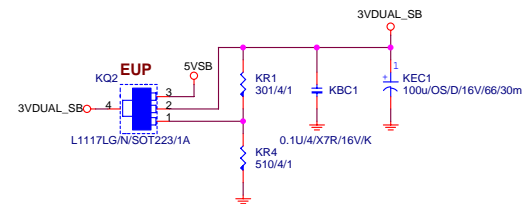
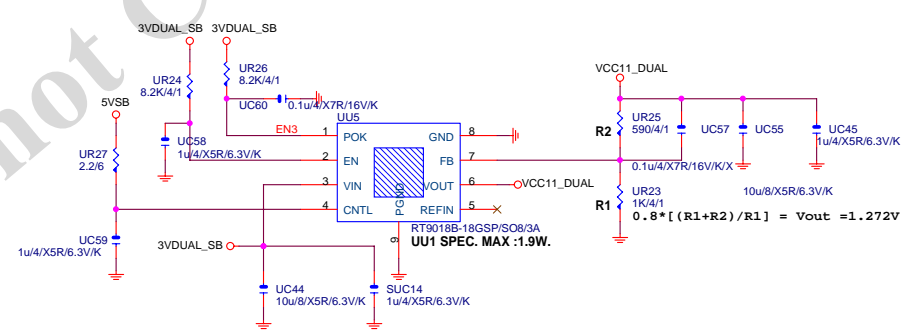
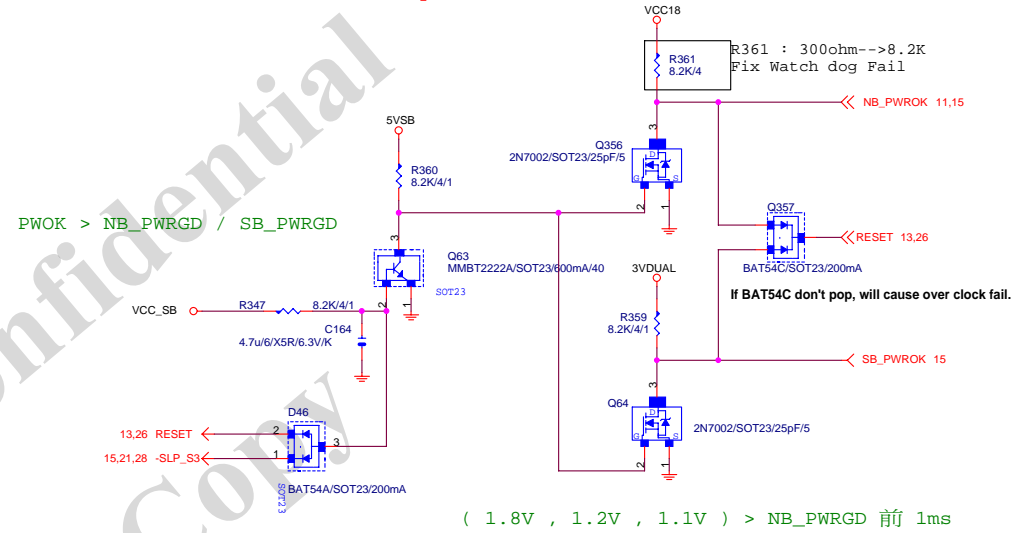
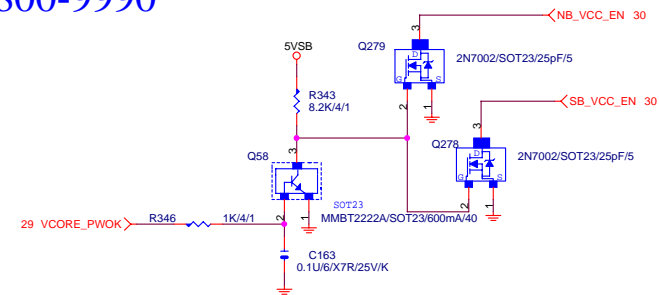
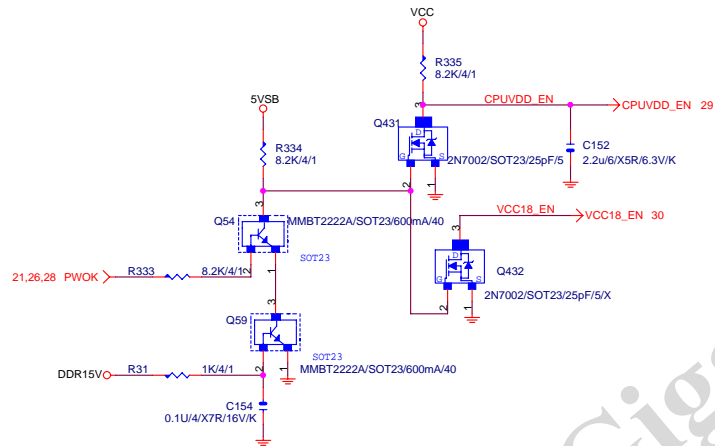
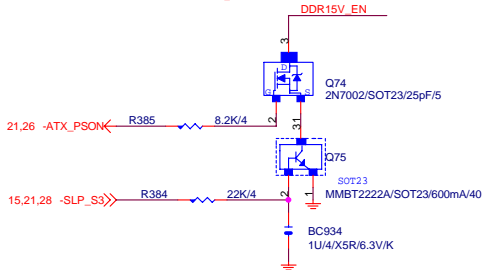
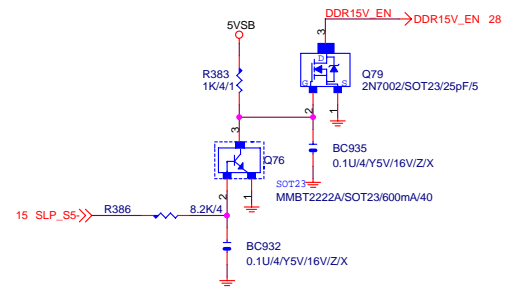
BH/2*5K10/BK/2.54/VA/COM

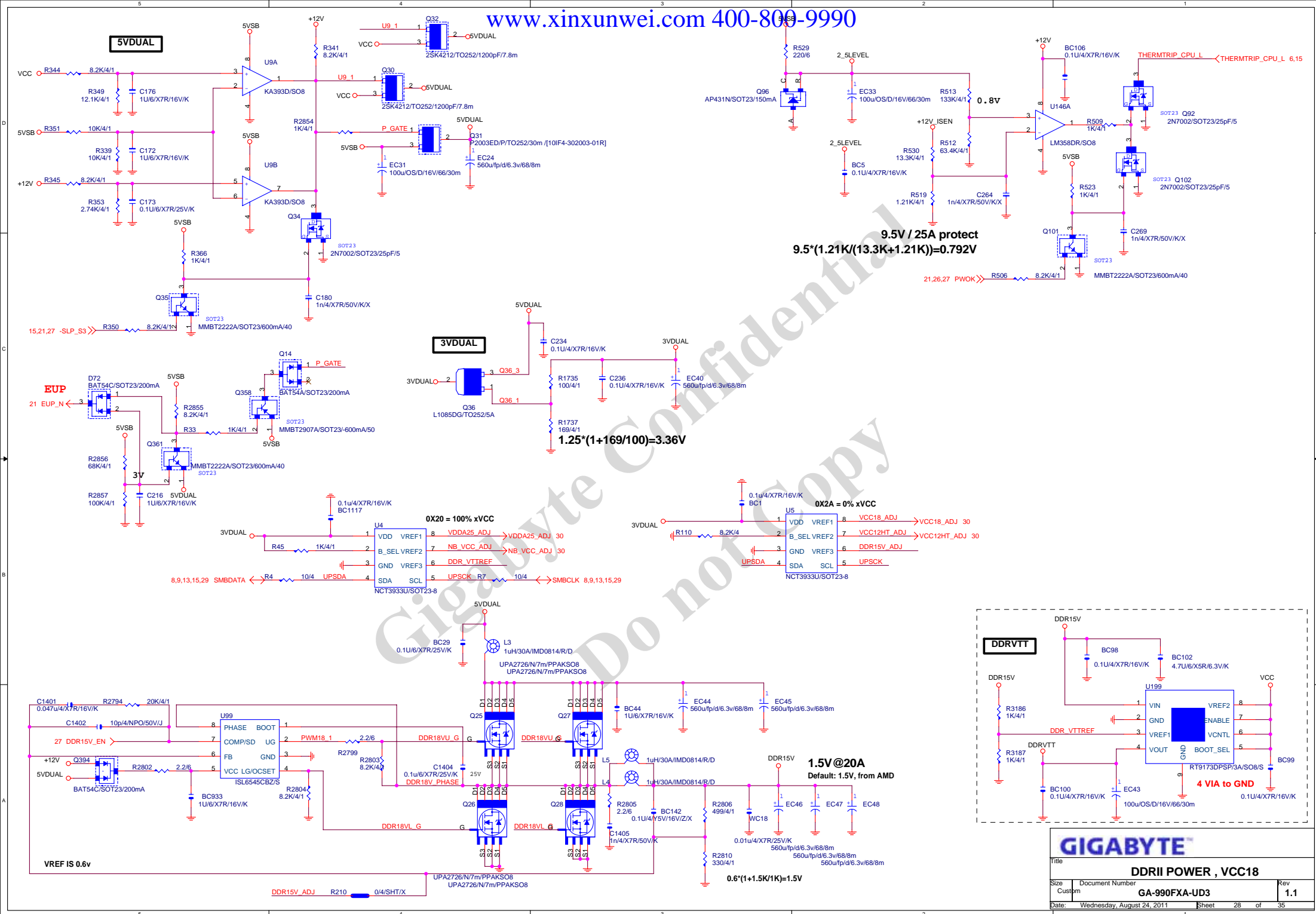
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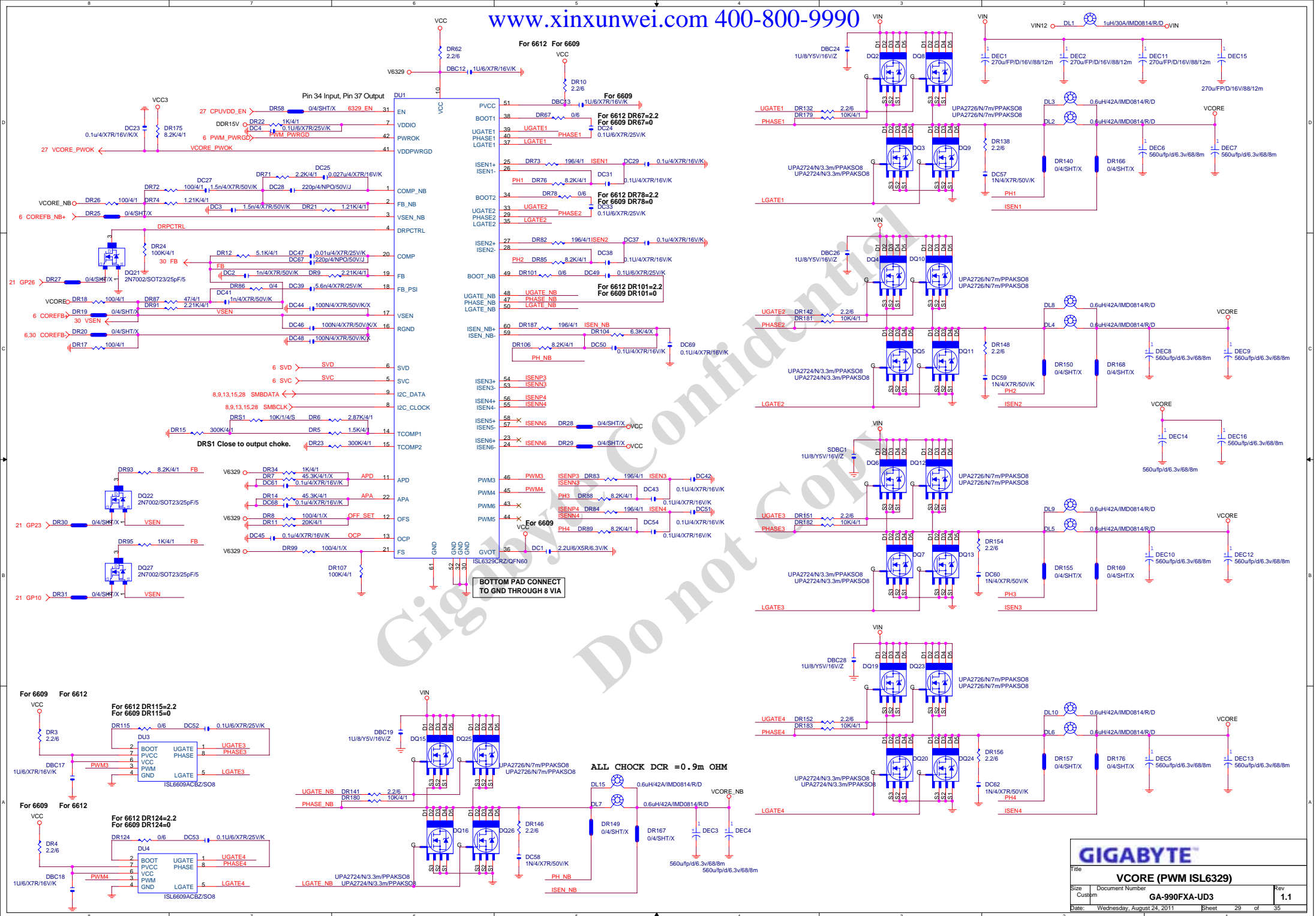
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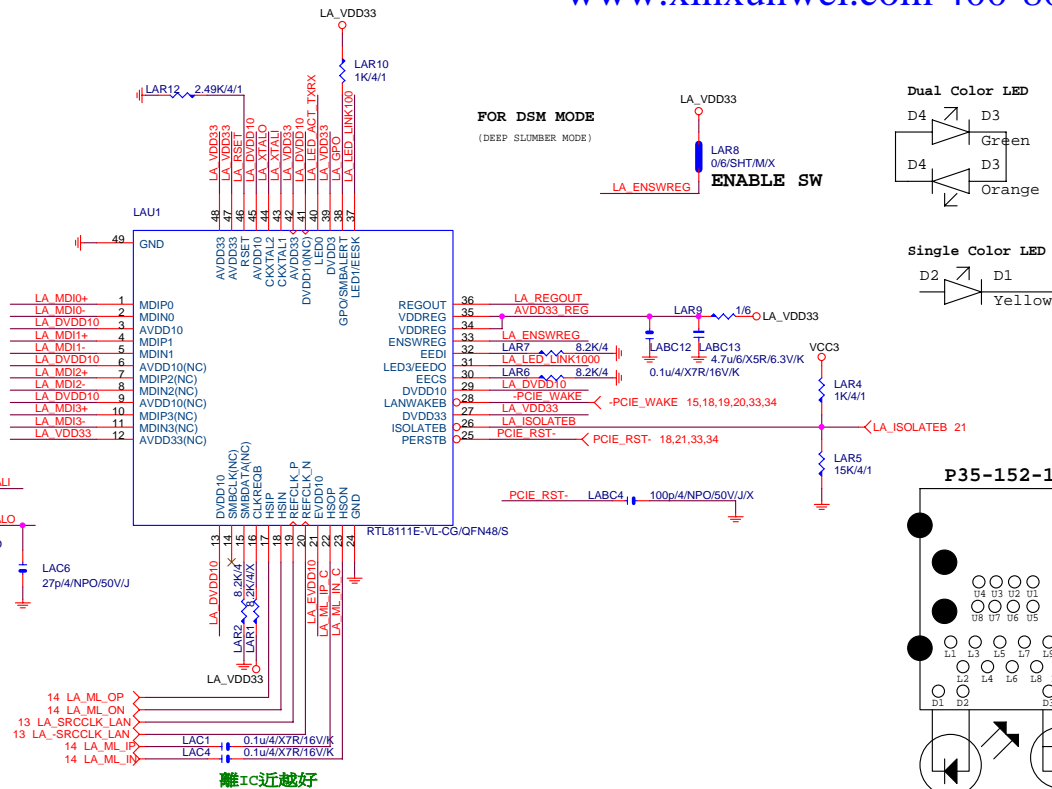




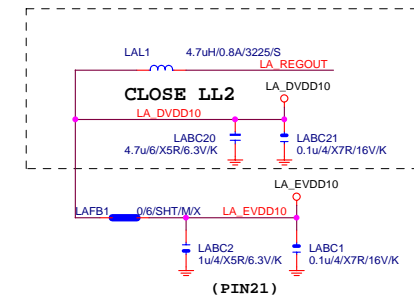
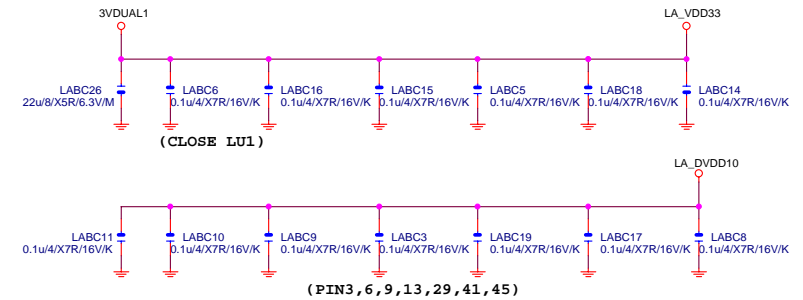
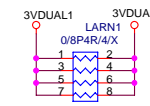
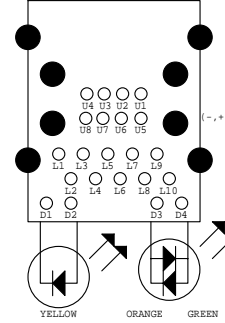
PCIE-1G LAN

Power domain chart

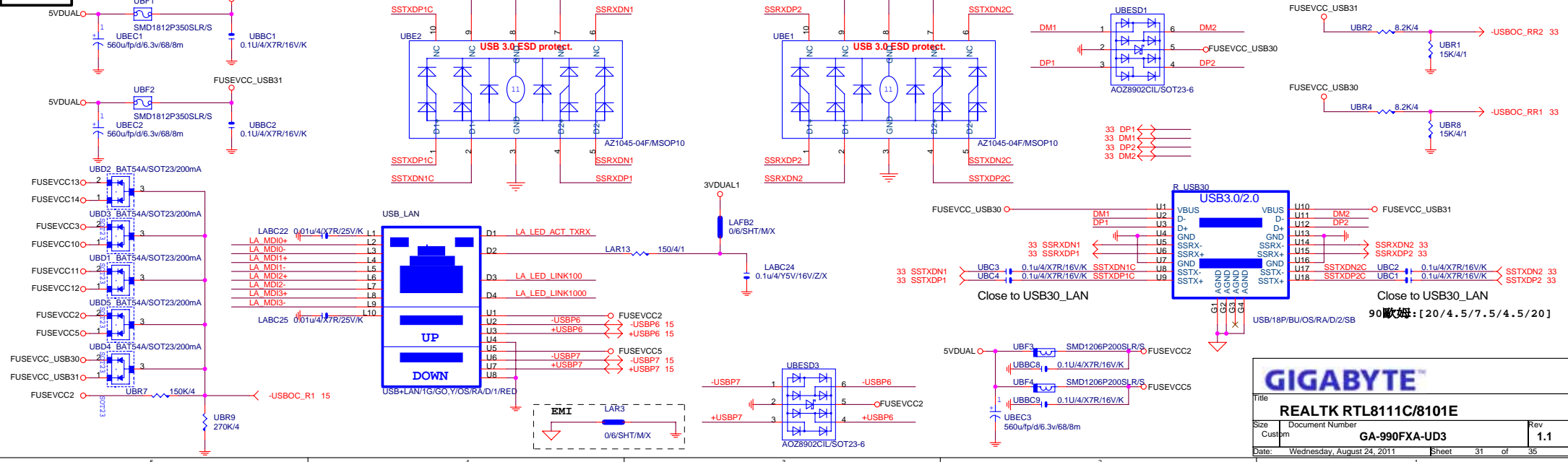
	RTL8111E
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

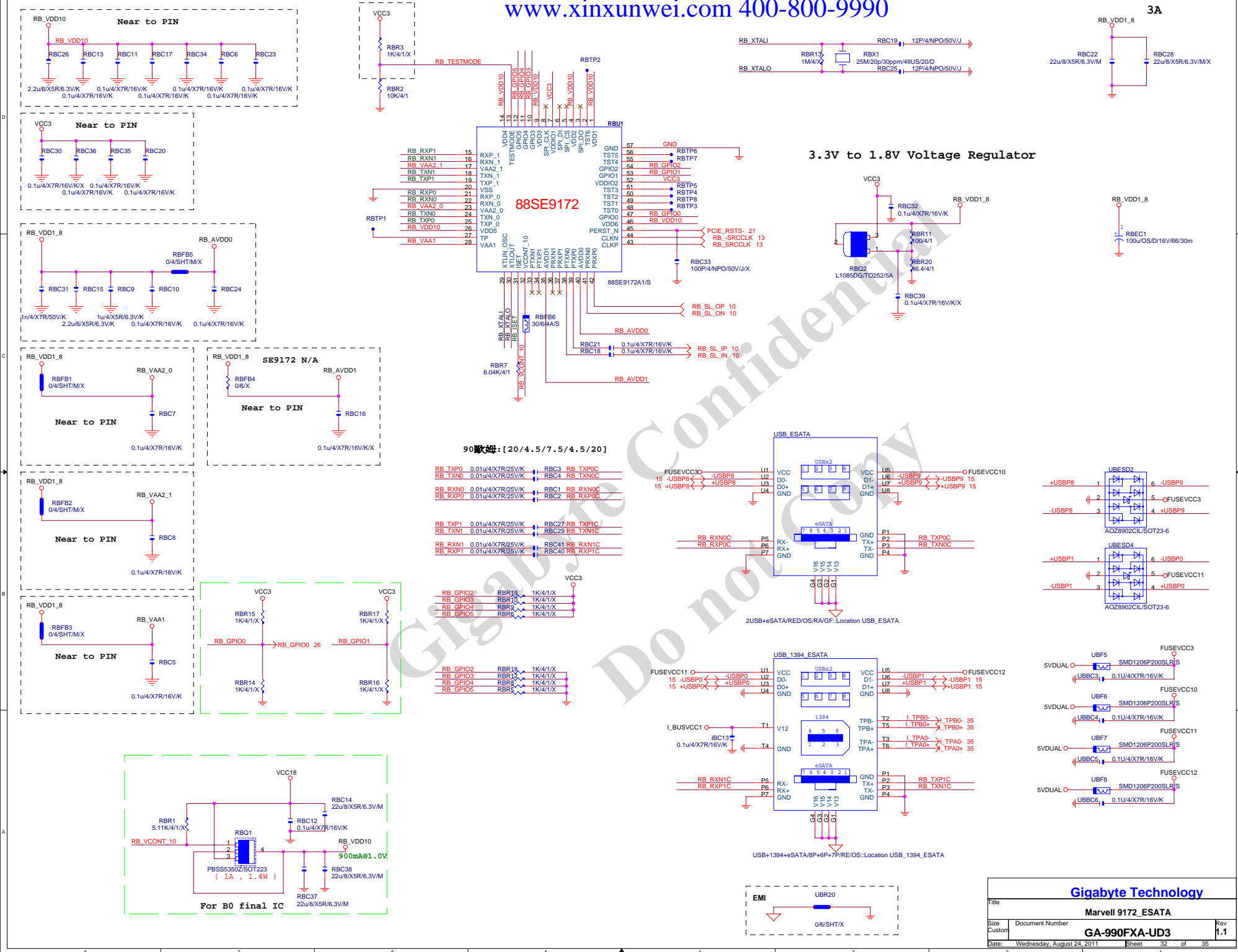


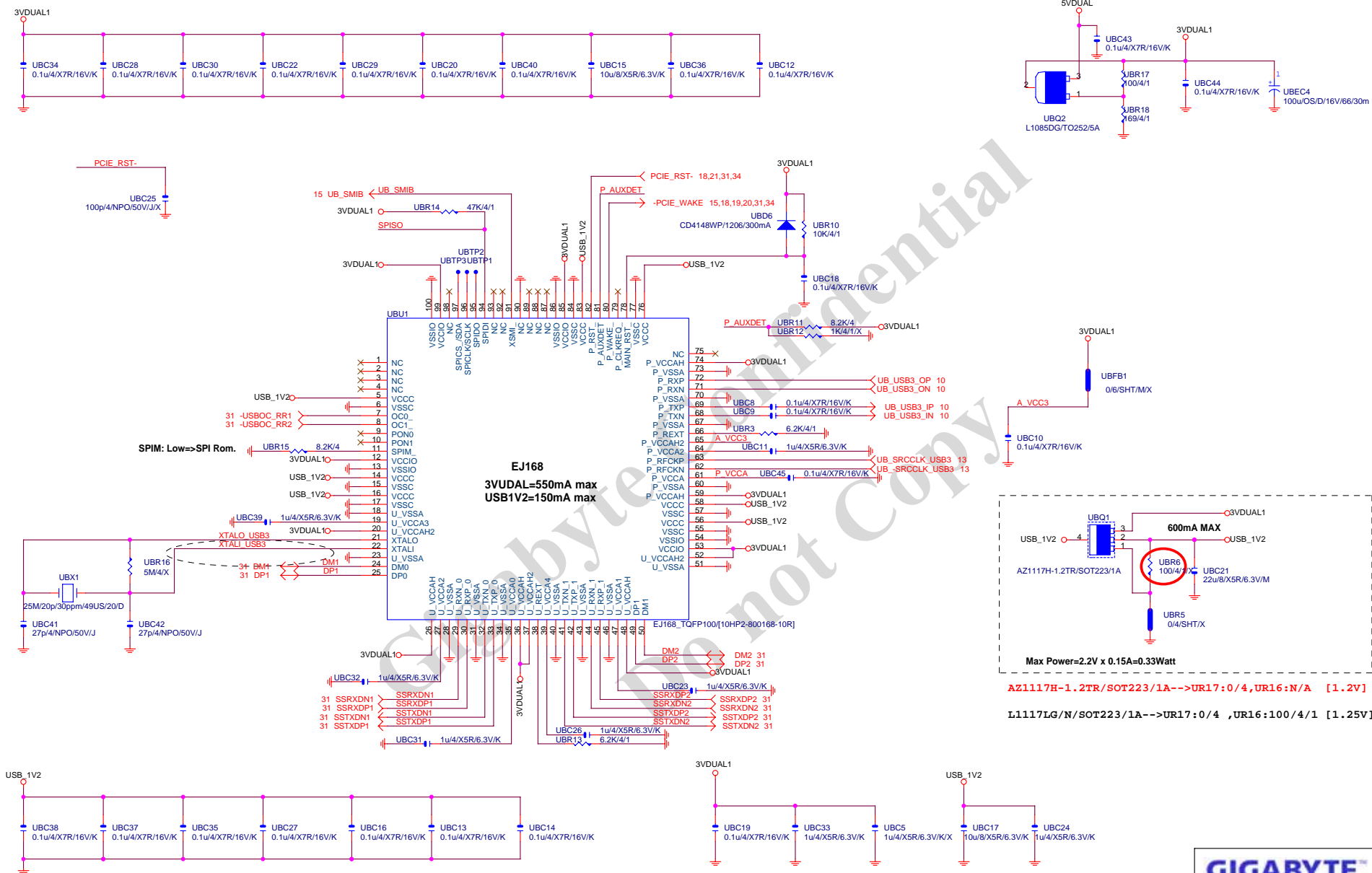
P35-152-19W9




USB_LAN

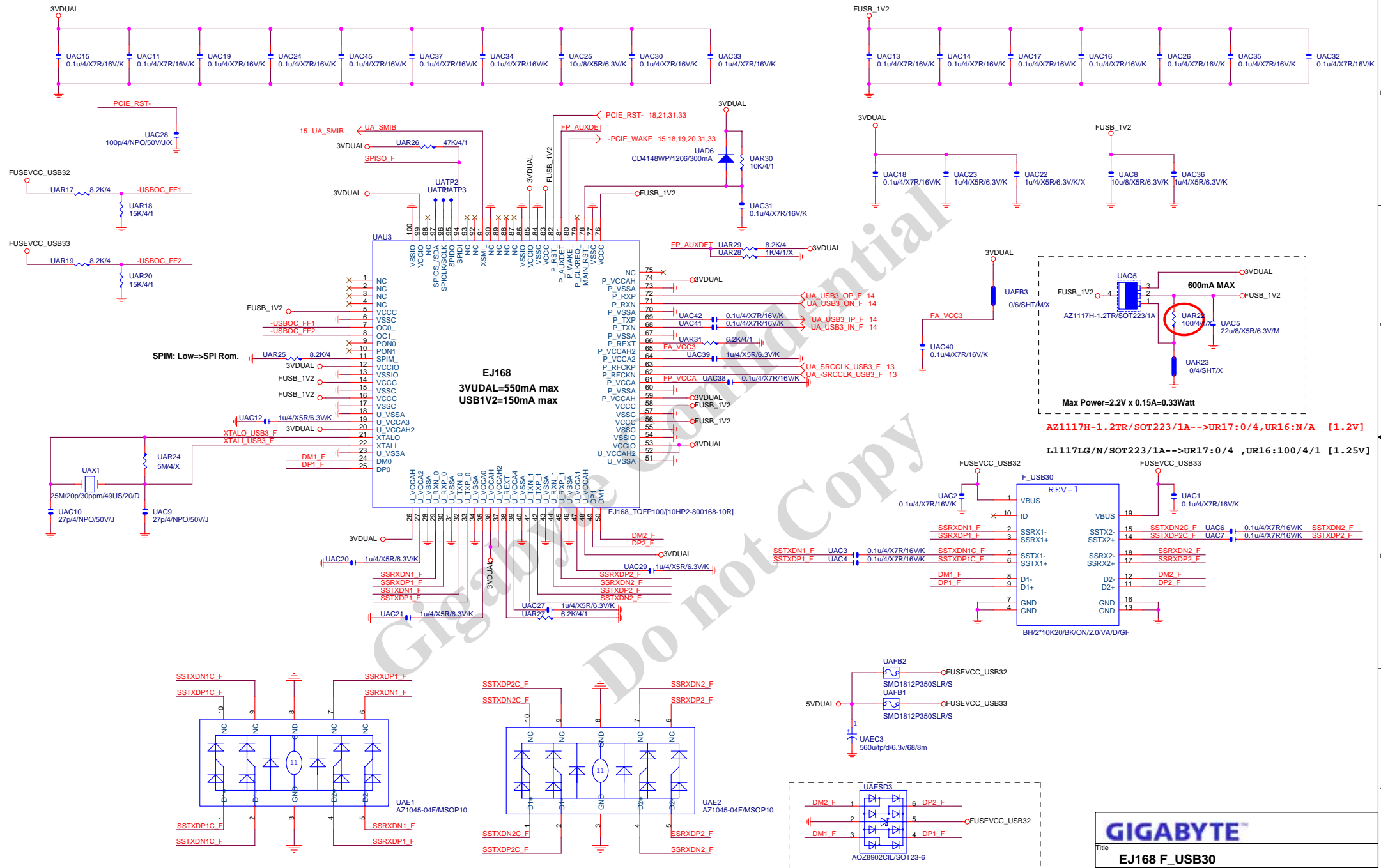


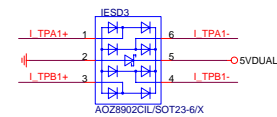
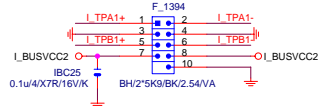
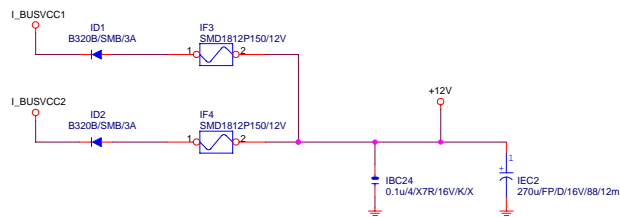
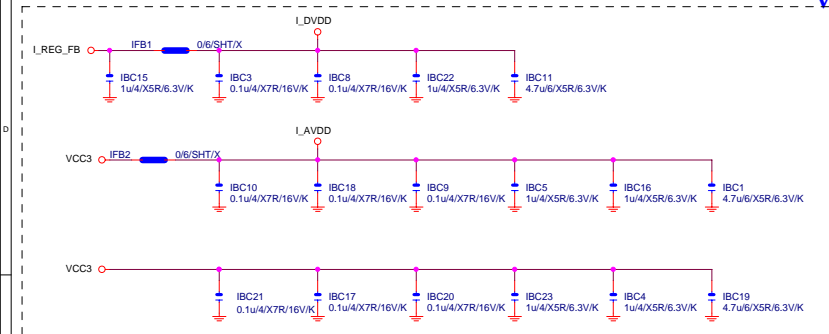




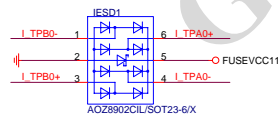
USB3.0 --> 5GHz
 BANDWIDTH=5GHz*(8b/10b)=4Gb/s=500MB/s

			
Title			
EJ168 R_USB30			
Size	Document Number	Rev	
Custom	GA-990FXA-UD3	1.1	
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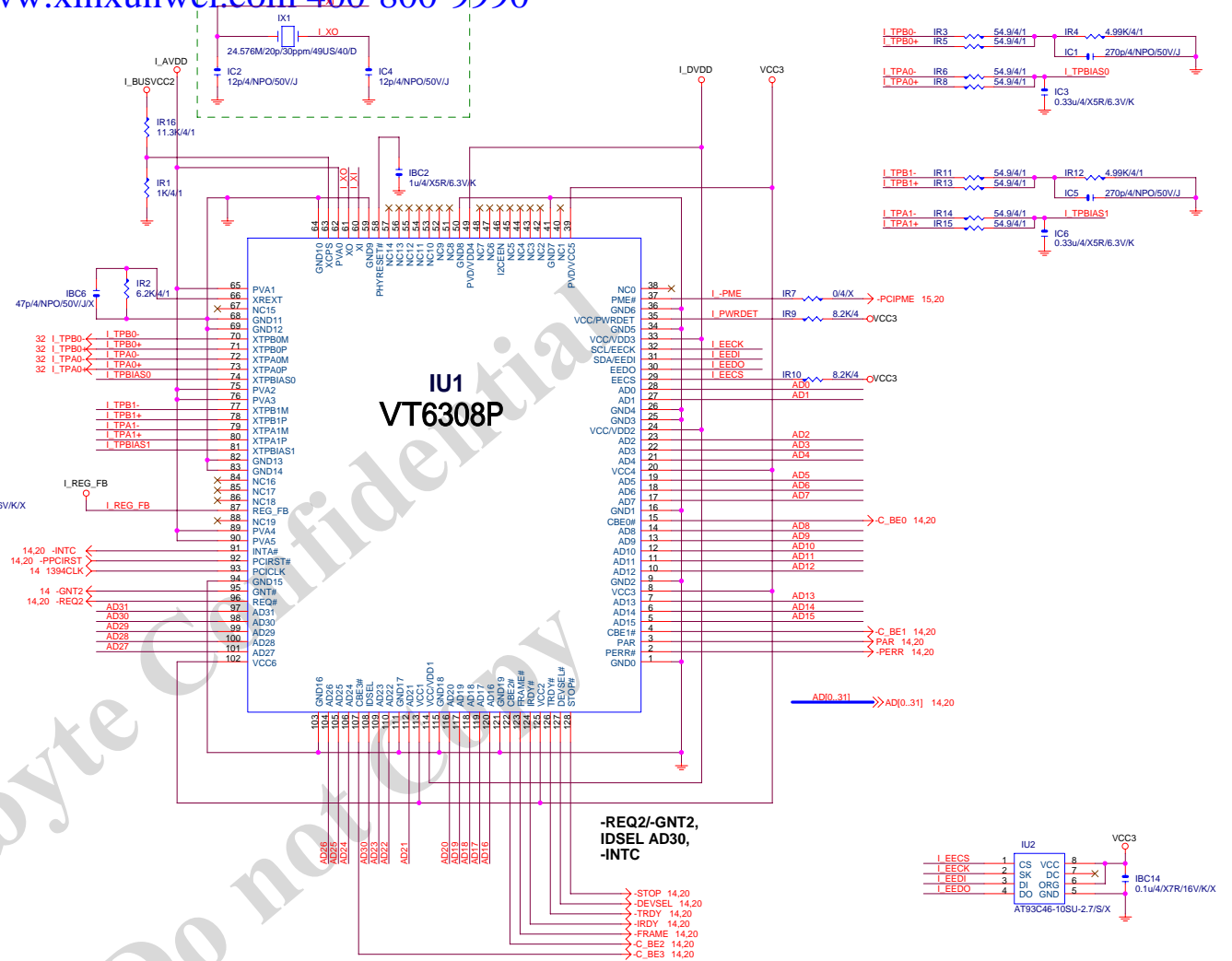




Place close to Header or connector

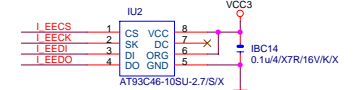


Place close to Header or connector



-REQ2/-GNT2,
IDSEL AD30,
-INTC

-STOP 14,20
-DEVSEL 14,20
-TRDY 14,20
-IRDY 14,20
-FRAME 14,20
-C_BE2 14,20
-C_BE3 14,20



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TI TSB43AB23 1394			
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